Application Note: SY56805A1

PoE Power Device

General Description

The SY56805A1 is a combined Power over Ethernet (PoE) powered device (PD) interface and primary side converter optimized specifically for isolated converter designs. The PoE interface supports the IEEE 802.3af standard as a 13W Type 1 powered device.

To achieve higher efficiency and better EMI performance, SY56805A1 drives Flyback converters in the Quasi-Resonant mode and adaptive PWM/PFM control. The flyback converter integrate a 150V, 0.14Ω MOSFET.

SY56805A1 features a detection signature pin which can also be used to disable the internal hotswap MOSFET. This allows the PoE function to be turned off during powered operation. Classification can be programmed to any of the defined Type 1 PD with a single resistor.

Features

- Power Up to 13W(input) PDs
- Supports the IEEE 802.3af Standard
- Primary Side Control
- QR-mode Operation for High Efficiency
- PWM/PFM Control for Higher Average Efficiency
- Adapter ORing Support
- 100 V, 0.45Ω Hotswap MOSFET
- Integrate 150V, 0.14Ω MOSFET for Converter
- RoHS Compliant and Halogen Free
- Compact Package: QFN5*5-32L

Applications

- IEEE 802.3af Compliant Devices
- Video and VoIP Telephones
- RFID Readers
- Multiband Access Points
- Security Cameras

Ordering Information

SY56805□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY56805A1QEC	QFN5*5-32L	---

Typical Applications

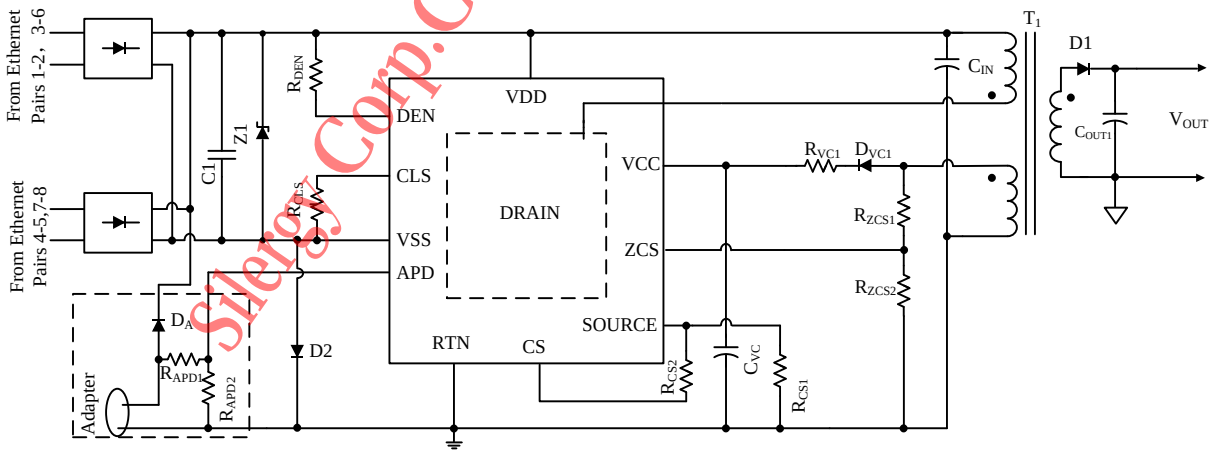
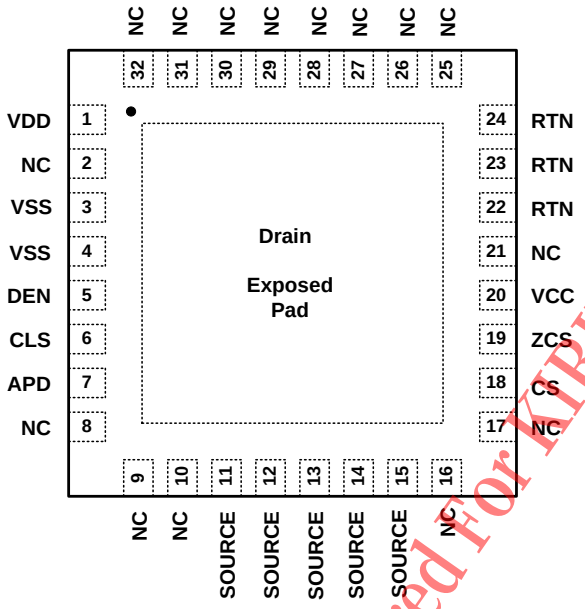


Figure 1. Schematic Diagram

Silergy Corp. Confidential Prepared For KIRTRON

© 2022 Silergy Corp. All Rights Reserved.

Pinout (top view)



(QFN5*5-32L)

Top Mark: EBF*xyz* (device code: EBF, ***x=year code, y=week code, z= lot number code***)

Name	Pin	Description
VDD	1	Connect to the positive PoE input power rail. VDD powers the PoE interface circuits. Bypass with a 0.1 µF capacitor and protect with a TVS.
VSS	3,4	Connect to the negative power rail derived from the PoE source.
DEN	5	Connect a 24.9 kΩ resistor from DEN to VDD to provide the PoE detection signature. Pulling this pin to VSS during powered operation causes the internal hotswap MOSFET to turn off.
CLS	6	Connect a resistor from CLS to VSS to program classification current. 2.5 V is applied to the program resistor during classification to set class current.
APD	7	Pull APD above 1.5 V disables the internal hotswap switch. This forces power to come from an external VDD-RTN adapter. Connect APD to RTN when not used.
SOURCE	11,12,13,14	Source of the internal power MOSFET.
SOURCE	15	Internal connected to the source of the internal power MOSFET， this pin can be floating.
CS	18	Current sense pin.
ZCS	19	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
VCC	20	DC/DC converter bias voltage.
RTN	22,23,24	RTN is the output of the PoE hotswap MOSFET.
Drain	Exposed Pad	Drain of the internal power MOSFET.
NC	others	Not connected.

Silergy Corp. Confidential Prepared For KRITRON

© 2022 Silergy Corp. All Rights Reserved.

Absolute Maximum Ratings (1)

Input voltage range [DEN, VDD, RTN (2)] to VSS ---------- -0.3-100V
Input voltage range [VDD, VCC] to RTN ---------- -0.3-100V
Input voltage range CLS (3) to VSS---------- -0.3- 5.5V
Input voltage range [ZCS, CS, APD] to RTN ---------- -0.3- 5.5V
Package Thermal Resistance (4)
QFN5*5-32L, θ_{JA} ---------- 25.13°C/W
QFN5*5-32L, θ_{JC} ---------- 16.85°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

Input voltage range [RTN, VDD] to VSS---------- 0- 72V
Input voltage range VDD to RTN ---------- 0- 72V
Input voltage range VCC to RTN ---------- 0- 18V
Junction Temperature Range ---------- -40°C to 125°C

Notes：

(1): Stresses beyond the “Absolute Maximum Ratings” may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2): I_{RTN}=0 for V_{RTN}>80V.

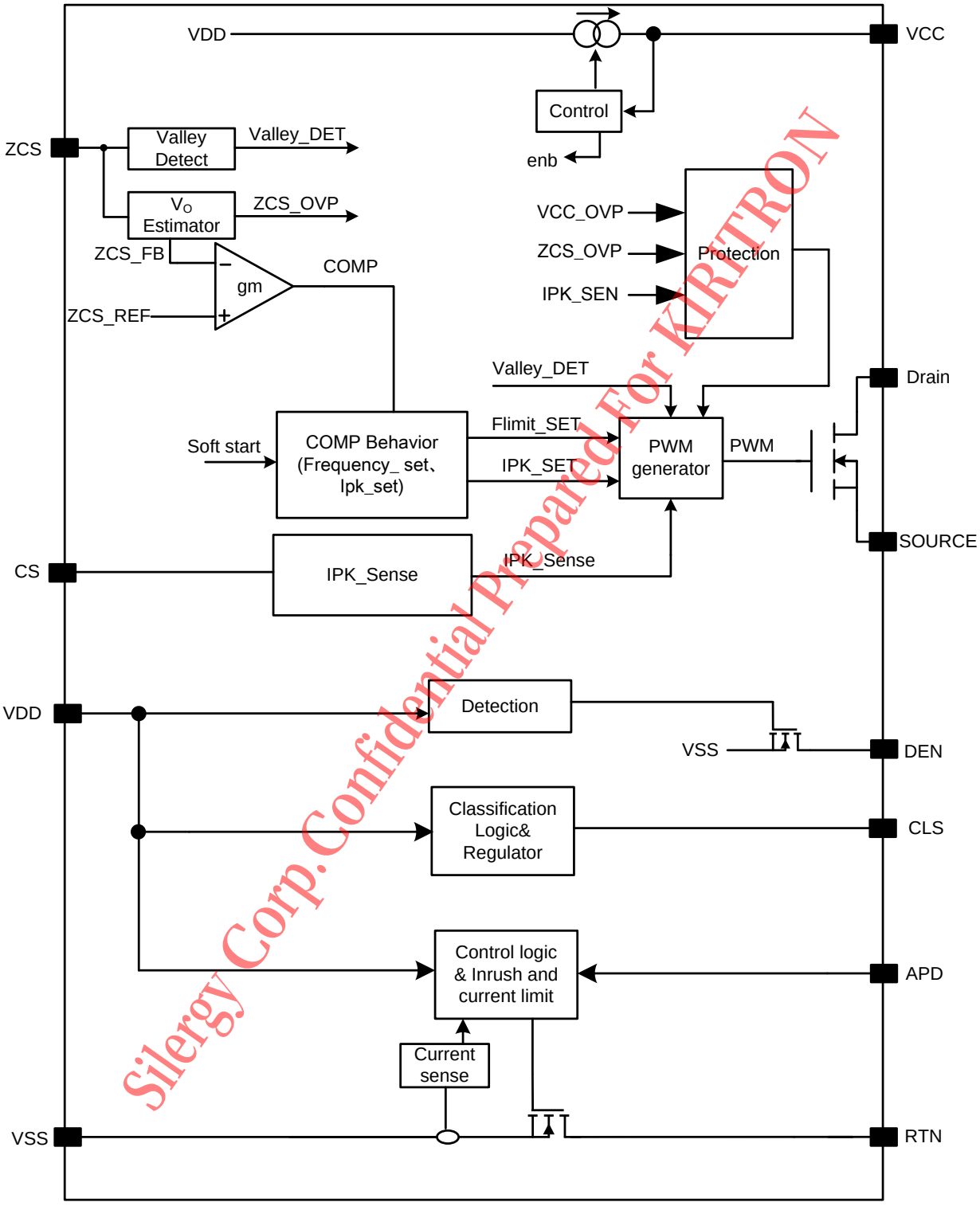
(3): Do not apply voltage to this pin.

(4): JESD 51-2，-5，-7，-8，-14 standard.

Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

Block Diagram



Silergy Corp. Confidential Prepared For KIRTRON

© 2022 Silergy Corp. All Rights Reserved.

Electrical Characteristics

(Unless otherwise noted: C_{VCC}=0.1 µF, R_{DEN}=24.9 kΩ, R_{CLS} open, V_{VDD}-V_{VSS} = 48 V, 9 V ≤ VCC≤ 18 V. Typical specifications are at 25°C.)

DC-DC Controller Section

VSS=RTN, all voltages referred to RTN.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC						
VCC Turn-on Threshold	V_{VCC_ON}		8.55	9	9.45	V
VCC UVLO Hysteresis	V_{VCC_HYS}			2.5		V
VCC SCP Threshold	V_{VCC_SCP}	V_{CC} falling	6.5	7	7.5	V
VCC OVP Voltage	V_{VCC_OVP}			22		V
Quiescent Current	I_Q		200	280	350	µA
Startup Current Source	I_{VCC}	V_{DD}=48V, V_{CC}=0V	0.5	1	2	mA
ZCS						
Voltage Reference	V_{ZCS_REF}		1.18	1.2	1.22	V
ZCS OVP Threshold	V_{ZCS_OVP}		1.35	1.45	1.55	V
Blanking Time for OFF Time	T_{OFF_MIN}		0.53	0.64	0.75	µs
CS						
Maximum Threshold Voltage	V_{LIMIT}		0.92	1.06	1.2	V
SWITCHING						
Max ON Time	T_{ON_MAX}			12		µs
Max OFF Time	T_{OFF_MAX}		400	550	700	µs
Maximum Switching Frequency	F_{MAX}		160	200	280	kHz
INTEGRATED MOSFET						
Breakdown Voltage	V_{BV}	V_{GS}=0V,I_{DS}=250µA	150			V
Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=12V,I_{DS}=0.1A		0.14		Ω
APD						
APD Threshold Voltage	V_{APD_EN}	V_{APD} rising	1.4	1.5	1.6	V
	V_{APD_H}	Hysteresis		0.3		V
APD Leakage Current		V_{APD}=5.5V			1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_J rising		150		°C
Hysteresis				20		°C

Silergy Corp. Confidential Prepared For KRITRON

© 2022 Silergy Corp. All Rights Reserved.

PD Interface Section

All voltages referred to VSS unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DETECTION	**DEN**	V_{VDD}= RTN=V_{SUPPLY} positive				
Detection Current		V_{VDD}=1.6V		60		μA
		V_{VDD}=10V		400		μA
Detection Bias Current		V_{VDD}=10V,float DEN, measure I_{SUPPLY}	4.5	7	10	μA
Hotswap Disable Threshold	V_{PD_DIS}		3	4	5	V
DEN Leakage Current		V_{DEN}=V_{VDD}=57V,measure I_{DEN}		0.1	5	μA
CLASSIFICATION	**CLS**	VDD= RTN=V_{SUPPLY} positive				
Classification Current	I_{CLS}	R_{CLS}=1270Ω		2		mA
		R_{CLS}=243Ω		10		mA
		R_{CLS}=137Ω		18		mA
		R_{CLS}=90.9Ω		28		mA
		R_{CLS}=63.4Ω		40		mA
Classification Regulator Lower Threshold	V_{CL_ON}	Regulator turns on, VDD rising	9	11	13	V
	V_{CL_H}	Hysteresis	1	2	3	V
Classification Regulator Upper Threshold	V_{CU_OFF}	Regulator turns off, VDD rising	21	22	23	V
	V_{CU_H}	Hysteresis	0.3	0.6	1	V
HOTSWAP MOSFET						
On Resistance				0.45	0.6	Ω
Current Limit				580		mA
Inrush Limit			50	60	80	mA
Leakage Current		V_{VDD}=V_{RTN}=100V, DEN=VSS			40	μA
UVLO						
UVLO Threshold	V_{UVLO_R}	VDD rising	34	35	36	V
	V_{UVLO_H}	Hysteresis		4.3		V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_J rising		150		°C
Hysteresis				20		°C

Silergy Corp. Confidential Prepared for KIRITRON

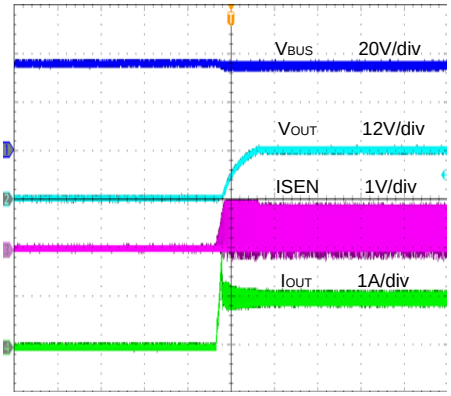
© 2022 Silergy Corp. All Rights Reserved.

Typical Performance Characteristics

(Test condition: input voltage: 37-57Vdc; output spec: 12Vdc/1A; Ambient temperature: 25±5 ℃; Ambient humidity:65±25%.)

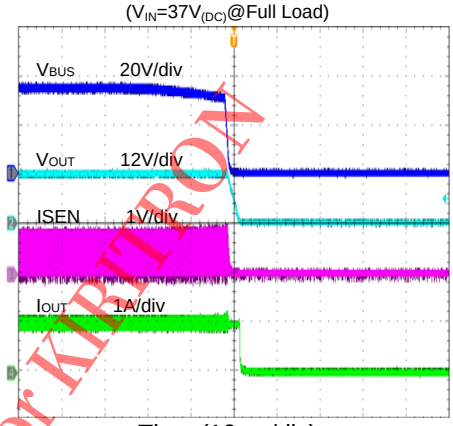
Startup

(V_{IN}=37$V_{(DC)}$@Full Load)



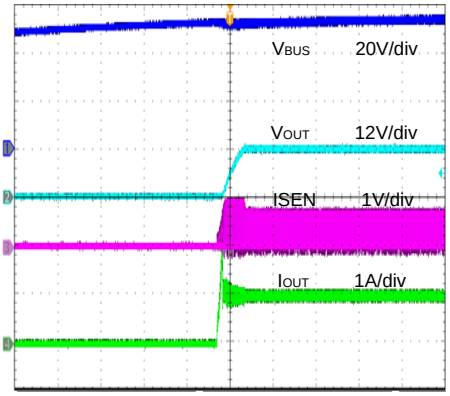
Shutdown

(V_{IN}=37$V_{(DC)}$@Full Load)



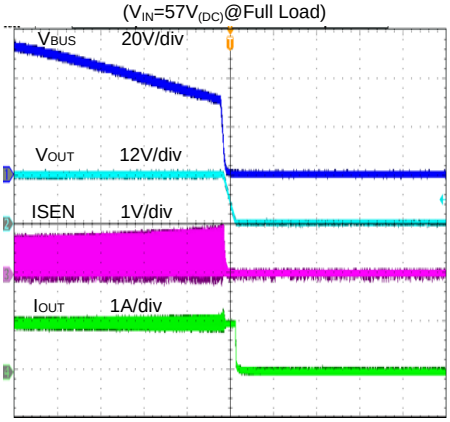
Startup

(V_{IN}=57$V_{(DC)}$@Full Load)



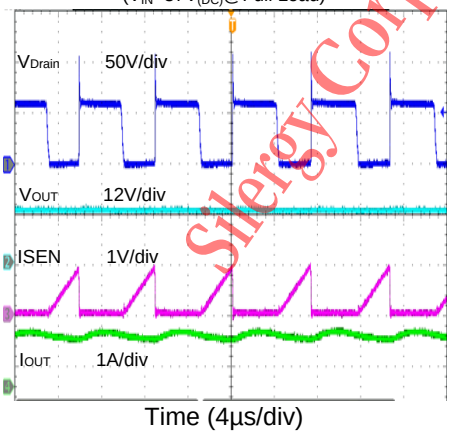
Shutdown

(V_{IN}=57$V_{(DC)}$@Full Load)



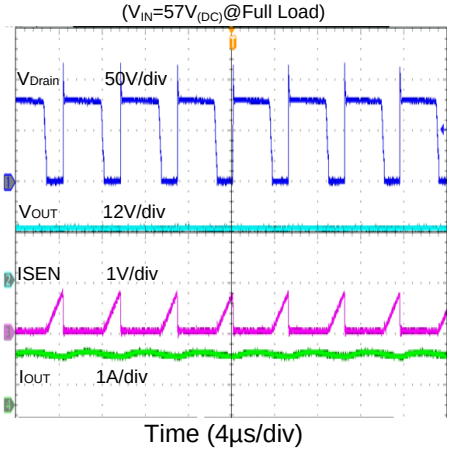
Steady

(V_{IN}=37$V_{(DC)}$@Full Load)



Steady

(V_{IN}=57$V_{(DC)}$@Full Load)

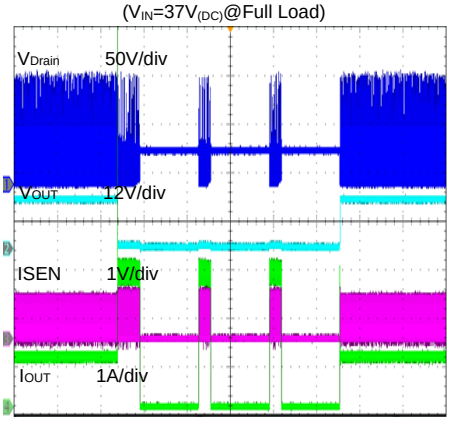


Silergy Corp. Confidential Prepared For KIRTRON

© 2022 Silergy Corp. All Rights Reserved.

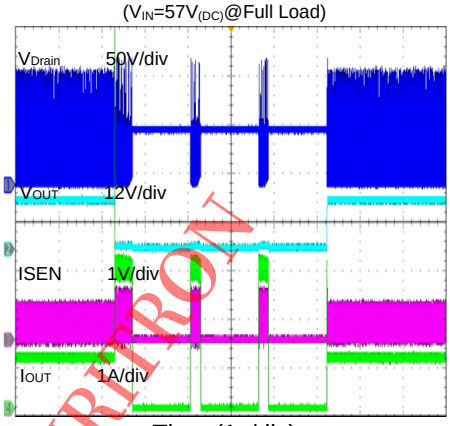
Short Circuit Protection

(V_{IN}=37$V_{(DC)}$@Full Load)

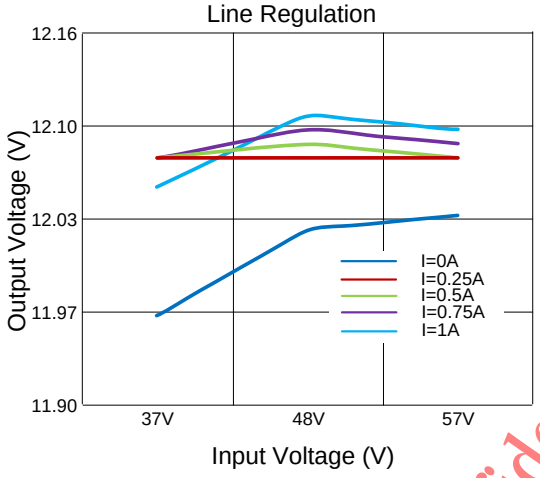


Short Circuit Protection

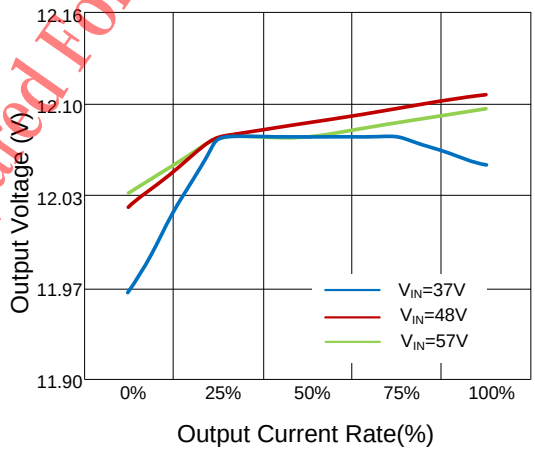
(V_{IN}=57$V_{(DC)}$@Full Load)



Line Regulation



Load Regulation



Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

Operation Principles

Protocol Section

Detection

In order to identify a device as a valid PD, the Power Sourcing Equipment (PSE) senses the Ethernet connection by applying two voltages in a range of 2.8 V to 10 V on the Ethernet cable and measuring the corresponding currents. An equivalent resistance is calculated using the ΔV/ΔI. During this phase, the PD must present a resistance between 23.75 kΩ and 26.25 kΩ. The value of the detection resistance has to be selected also taking into account the typical drop in voltage of the diode bridges. The typical value that can be used in most case is 24.9 kΩ.

Classification

In the classification mode, the PSE will classify the PD for one of five power levels or classes. This allows the PSE to efficiently manage power distribution. The five different classes is shown in Table 1, it determine the class the PD must advertise. An external resistor (R_{CLS}) connected from CLS to VSS sets the classification current. The PSE may disconnect a PD if it draws more than its stated Class power. During hardware Classification, the PSE presents a fixed voltage between 15.5 V and 20.5 V to the PD, which in turn draws a fixed current set by R_{CLS}. PD current is measured by the PSE to determine which of the five available classes is advertised (see Table 1). The SY56805A1 disables classification while the input voltage is above 22V to avoid excessive power dissipation. If the PD thermal limit is trigger or when APD or DEN is active, the CLS reference voltage will be turned off .

Table 1. Class Resistor Selection

Class	Power at PD(W)	Class current (mA)	Resistor
0	0.44~12.95	0~4	1270
1	0.44~3.84	9~12	243
2	3.84~6.49	17~20	137
3	6.49~12.95	26~30	90.9
4	-	36~44	63.4

Inrush and Operational Current Limit

Once the classification is successfully completed, the PSE will rise its voltage, when the input voltage is above UVLO turn on threshold(35V), the hotswap switch is turned on, and the input capacitor is charged with a low current (inrush current) limit until the voltage across hotswap switch is sufficiently low, indicating the switcher supply capacitor is almost completely charged. Once the inrush current falls and the RTN drops to nearly zero, the PD current limit switches to the operational level.

Adapter Power Input

In some applications, it is desirable to power the PD from an auxiliary power source such as a wall adapter. The SY56805A1 supports forced operation from either of the power sources. Figure 1 illustrates the recommended connection of the adapter power to PD.

The hot-swap switch is disabled while the adapter is used to pull APD high (up to 1.5V), blocking the PoE source from powering the output.

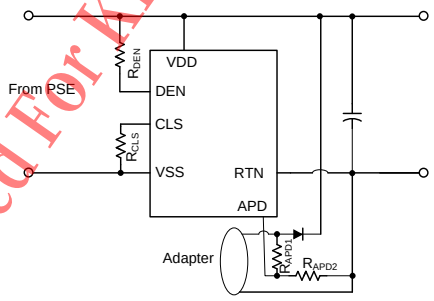


Fig.1 Adapter Power Input

DC-DC Controller Operation

Start-up Operation

After DC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VCC and RTN pins, C_{VCC}, is charged up by the BUS voltage through internal start up circuit. Once V_{VCC} rises up to V_{VCC_ON}, the internal blocks starts the operation. V_{VCC} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy. To avoid triggering V_{VCC_SCP} threshold during start-up, the VCC bypass capacitor should be large enough to maintain V_{VCC} above V_{VCC_SCP}(7V typical). The start-up procedure is divided into two sections, as shown in Fig.2: t_{STC} is the C_{VCC} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

Silergy Corp. Confidential Prepared For KINTRON

© 2022 Silergy Corp. All Rights Reserved.

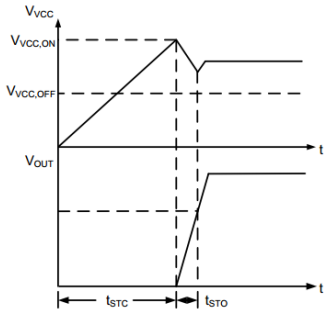


Fig.2 Start up

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

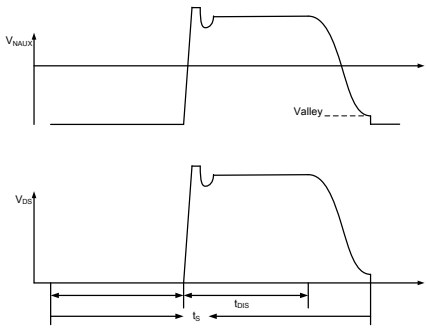


Fig.3 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. ZCS pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Output Voltage Control

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

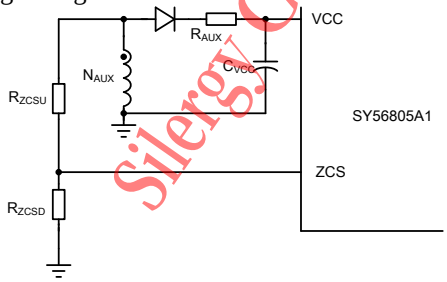


Fig.4 ZCS pin connection

As shown in Fig.5, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (1)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{ZCS\_REF}}{V_{OUT}} = \frac{R_{ZCSD}}{R_{ZCSU} + R_{ZCSD}} \times \frac{N_{AUX}}{N_S} \quad (2)$$

Where V_{ZCS_REF} is the internal voltage reference.

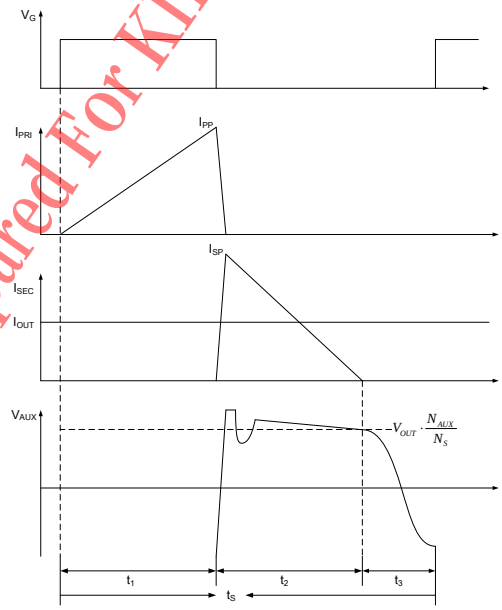


Fig.5 Auxiliary winding voltage waveforms

Fault Protection Modes

ZCS Pin Short Protection

The SY56805A1 has a protection against faults caused by a shorted ZCS pin. During start-up, the voltage on the ZCS pin is monitored. In normal situations, the voltage on the ZCS pin reaches the sense protection trigger level. When the ZCS voltage does not reach this level, the ZCS pin is shorted and the protection is activated. The IC stops switching and discharge the VCC voltage. Once V_{VCC} is below V_{VCC_OFF}, the IC will shut down and be charged again by VDD.

CS pin Short Protection

The SY56805A1 has a protection against the faults caused by shorting CS pin to RTN. During start-up, the voltage on the CS pin is monitored. If the V_{CS} does not

Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

exceed 150mV after 2.5μS, the protection will be triggered, the IC stops switching and discharge the VCC voltage. Once V_{VCC} decreases below V_{VCC_OFF}, the IC will shut down and the VCC will be charged again by VDD.

Output Over Voltage Protection

When the ZCS pin signal exceeds 1.45V, reflecting an output over-voltage condition, SY56805A1 will stop switching and discharge the VCC voltage. Once V_{VCC} is below V_{VCC_OFF}, the IC will shut down and the VCC will be charged again by VDD.

VCC Over Voltage Protection

When the VCC voltage exceeds VVCC_OVP threshold, SY56805A1 will stop switching and discharge the VCC voltage. Once VVCC is below VVCC_OFF, the SY56805A1 will shut down and the VCC will be charged again by VDD.

Short Circuit Protection (SCP)

The SCP will be triggered when the VCC is falling below $V_{VCC\text{-}SCP}$ (7V typical) and the voltage of internal comp is up to 2V.

When the IC starts up with heavy load, or the output current is getting heavier and heavier during normal operation, or output is shorted to ground, the VCC voltage will decrease and internal COMP will be high. Once V_{VCC} is below V_{VCC_SCP}, IC will shut down immediately, VCC will be charged again by VDD. To avoid thermal rising risk, a digital counter is adopted. When VCC has reached V_{VCC_ON}, the counter will plus 1. When the counter has reached number 8, SCP flag signal will be reset. Meanwhile, IC will try to start up again.

In order to guarantee SCP function is not affected by voltage spike of auxiliary winding, a filter resistor R_{AUX} is needed.

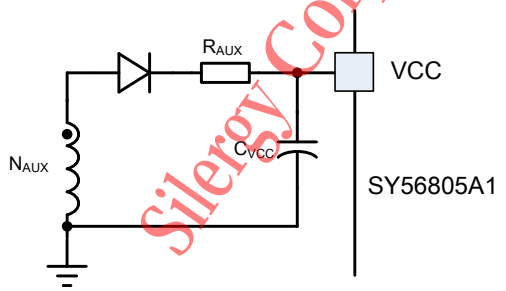


Fig. 6 Filter resistor R_{AUX}

Power Device Design

MOSFET and DIODE

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = V_{DC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (3)$$

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT} \quad (4)$$

Where V_{DC_MAX} is maximum input DC voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (5)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (6)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (7)$$

$$I_{D\_AVG} = I_{OUT} \quad (8)$$

Where $I_{P\_PK\_MAX}$ and $I_{P\_RMS\_MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (9)$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.8.

Silergy Corp. Confidential Prepared For KRITRON

© 2022 Silergy Corp. All Rights Reserved.

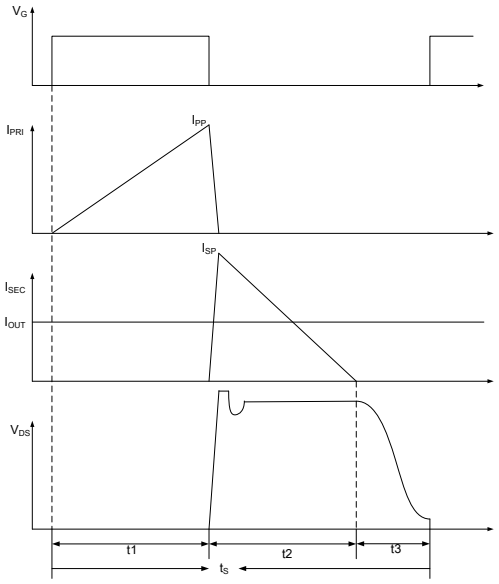


Fig.7 switching waveforms

When the operation condition is with minimum input DC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (10)$$

(b) Preset minimum frequency f_{S_MIN}

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (11)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (12)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET; η is the efficiency; P_{OUT} is rated full load power.

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (13)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (14)$$

$$t_S = \frac{1}{f_{S\_MIN}} \quad (15)$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (16)$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (17)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \cdot I_{P\_PK\_MAX} \cdot \sqrt{\frac{t_2}{t_S}} \quad (18)$$

Transformer Design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB
ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (19)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (20)$$

Silergy Corp. Confidential Prepared For KRITRON

© 2022 Silergy Corp. All Rights Reserved.

(e) compute auxiliary turn N_{AUX}

$$N_{AUX}=N_S\times\frac{V_{VCC}}{V_{OUT}} \quad (21)$$

Where V_{VCC} is the working voltage of VCC pin (10V~15V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

RCD Snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT} \quad (22)$$

Where N_{PS} is the turns ratio of the flyback transformer; V_{OUT} is the output voltage; V_{D_F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss,

$$R_{RCD}=\frac{(N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S)^2}{P_{RCD}} \quad (23)$$

The C_{RCD} is related with the voltage ripple of the snubber ΔV_{C_RCD}:

$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}\times f_S\times\Delta V_{C\_RCD}} \quad (24)$$

CLS Resistor Selection

A resistor from CLS to V_{SS} programs the classification current per the IEEE standard. The PD power ranges and corresponding resistor values are listed in following table. The power assigned should correspond to the maximum average power drawn by the PD during operation. SY56805A1 supports class 0-3 power levels.

Table2. Class Resistor Selection

Class	Power at PD		Resistor
	Minmum (W)	Maximum (W)	
0	0.44	12.95	1270
1	0.44	3.84	243
2	3.84	6.49	137
3	6.49	12.95	90.9

APD Resistor Selection

APD forces power to come from an external adapter connected from VDD to RTN by opening the hotswap switch. Select the APD divider resistors per Equation (22) where V_{ADPTR_ON} is the desired adapter voltage that enables the APD function as adapter voltage rises.

$$R_{APD1}=R_{APD2}\times(V_{APDTR\_ON}-V_{APDEN})/V_{APDEN}$$
$$V_{APDTR\_OFF}=\frac{R_{APD1}+R_{APD2}}{R_{APD2}}\times(V_{APDEN}-V_{APDH}) \quad (22)$$

DEN Resistor Selection

The standard specifies a detection signature resistance, R_{DEN} between 23.7 kΩ and 26.3 kΩ. Connect a 24.9kΩ resistor from DEN to VDD to provide the PoE detection signature.

VDD to VSS ESD Protection

Voltage transients caused by surge or other special applications can occur, a TVS (D1, see in Fig.8) must limit this voltage to be within the absolute maximum ratings. The TVS such as SMBJ58A can be used. A TVS with negative resistance characteristic is not recommended. A Schottky diode (D2 on the Fig.8) such as PT3L100F-A is required between VSS and RTN for application design.

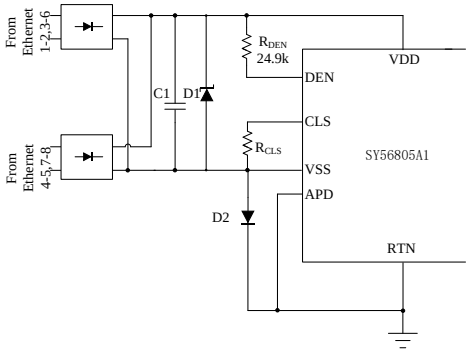


Fig.8 VDD to VSS ESD protection

Silergy Corp.Confidential Prepared For XPTRON

© 2022 Silergy Corp. All Rights Reserved.

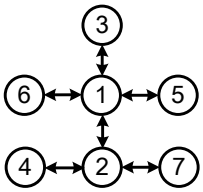
Input Bypass Capacitor Selection

The standard specifies an input bypass capacitor of 0.05 μF to 0.12 μF. Typically a 0.1 μF, 100V ceramic capacitor between VDD and VSS(C1 on the Fig.8) is used while the input power source is only PSE (C2 not connnect).

If the external adapter is also used to power the device, one capacitor C1 between VDD and VSS, and one capacitor C2 between RTN and VSS is both recommended to be connected. The typical value of C1 and C2 is both recommended to be 0.047uF/100V.

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.
(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.
(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS capacitor.
Ground ②: ground of bias supply capacitor.
Ground ③: ground node of auxiliary winding.
Ground ④: ground node of divider resistor.
Ground ⑤: primary ground node of Y capacitor.
Ground ⑥: ground node of current sample resistor.
Ground ⑦: ground of IC GND.

(d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.
(e) Loop of `Source pin – current sample resistor – GND pin` should be kept as small as possible.
(f) The resistor divider connected to ZCS pin is recommended to be put beside the IC.

Design Notice

1. At no load secondary side diode freewheeling time should be more than T_{OFF_MIN}.
2. VCC voltage prefer to larger than 10V for all conditions.
3. At heavy load, the peak-to-peak voltage at the ZCS pin should be less than approximately 100mV after. T_{OFF_MIN} time. This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
4. R_{ZCSU} is the upper resistor of the divider. Normally, its value is recommended between 30kΩ~91kΩ.
5. In order to ensure the loop stability, the output capacitor should be selected properly. On the other hand, switching frequency ripple should also be considered. If the switching frequency ripple is too large, increase the capacitance of Cout properly or use low ESR capacitor.

Silergy Corp. Confidential Prepared for KRIPRON

© 2022 Silergy Corp. All Rights Reserved.

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{DC}	37V~57V	V_{OUT}	12V
I_{OUT}	1A	η	82%

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
V_{DC_MIN}	37V	V_{DC_MAX}	57V
ΔV_S	50V	$V_{MOS-(BR)DS}$	150V
P_{OUT}(max)	12W	V_{D_F}	1V
C_{Drain}	60pF	f_{S_MIN}	150kHz

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$

$$= \frac{150V \times 0.9 - 57V - 50V}{12V + 1V}$$

$$= 2.15$$

N_{PS} is set to

$N_{PS} = 2$

(b)$f_{S,MIN}$ is preset

$f_{S\_MIN} = 150kHz$

(c) Compute inductor L_M and maximum primary peak current $I_{P,PK,MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times \left(V_{DC\_MIN} \frac{N_{PS} V_O}{N_{PS} V_O + V_{DC\_MIN}} \right)}$$

$$= \frac{2 \times 12W}{0.82 \times (37V \times \frac{2*12V}{2*12V + 37V})}$$

$$= 2.01A$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$

$$= \frac{2 \times 12W}{0.82 \times (2.01A)^2 \times 150KHz}$$

$$= 48.78\mu H$$

Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

Set: L_M=48μH

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC\_MIN}} = \frac{48\mu H \times 2.01A}{37V} = 2.607\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{48\mu H \times 2.01A}{2 \times (12V + 1V)} = 3.711\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{48\mu H \times 60pF} = 0.168\mu s$$

$$t_S = t_1 + t_2 + t_3 = 2.607\mu s + 3.711\mu s + 0.168\mu s = 6.486\mu s$$

(e) Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 2.01A \times \sqrt{\frac{2.607\mu s}{6.486\mu s}} = 0.736A$$

(f) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 2.01A = 4.02A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} = 2 \times \frac{\sqrt{3}}{3} \times 2.01A \times \sqrt{\frac{3.711\mu s}{6.486\mu s}} = 1.756A$$

#3. Select secondary power diode

Refer to Power Device Design

Known conditions at this step			
V_{DC_MAX}	57V	N_{PS}	2
V_{OUT}	12V	V_{D_F}	1V

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT}$$
$$= \frac{57V}{2} + 12V$$
$$= 40.5V$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 2.01A = 4.02A$$

$$I_{D\_AVG} = 1A$$

#4. Set current sense resistor to achieve ideal output current

Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

Known conditions at this step			
N_{PS}	2		
V_{LIMIT}	1V	$I_{OUT,LIM}$	1.3A

The current sense resistor is

$$R_S = \frac{V_{LIMIT}}{I_{P\_PK\_MAX}} = \frac{1V}{2.01A} = 0.498\Omega$$

Set Rs

$Rs=0.5\Omega$

#5. Set ZCS pin

Refer to V_{OUT}

First identify R_{ZCSU} need for line regulation.

Parameters Designed			
R_{ZCSU}	56kΩ		

Then compute R_{ZCSD}

Conditions			
V_{OUT}	12V	V_{ZCS_REF}	1.2V
R_{ZCSU}	56kΩ	N_S	9
N_{AUX}	9		

$$R_{ZCSD} = \frac{R_{ZCSU}}{\frac{V_{OUT} \times N_{AUX}}{(V_{ZCS\_REF}+0.1V) \times N_S} - 1} = \frac{56K}{(\frac{12V \times 9}{(1.2V+0.1) \times 9} - 1)} = 6.8K$$

Set R_{ZCSD}
(Note: In consideration of the propagation delay of internal circuit, a 0.1V is added to V_{ZCS_REF} for compensation.)

$R_{ZCSD}=6.8k\Omega$

#6. Set DEN pin
Connect a 24.9kΩ resistor from DEN to VDD

#7. Set CLS pin
Connect a 1.27kΩ resistor from CLS to VSS

#9. Final result

Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

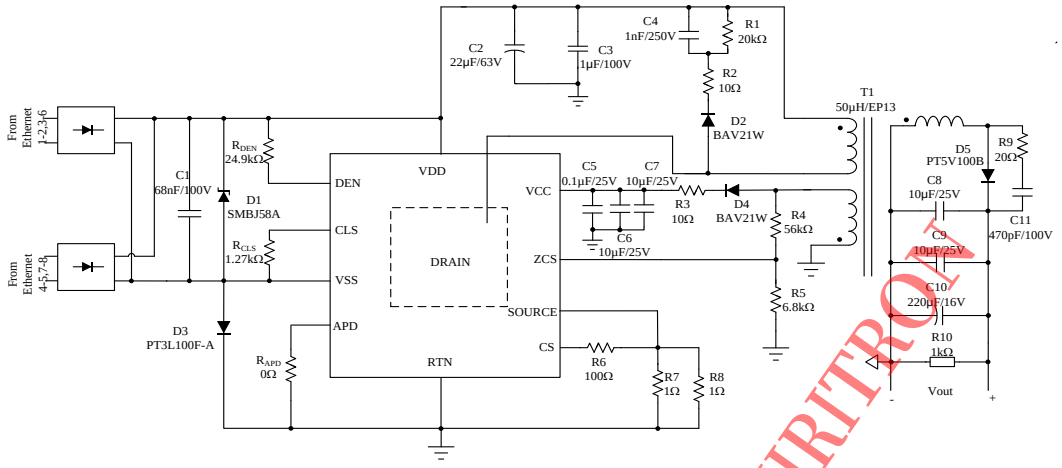
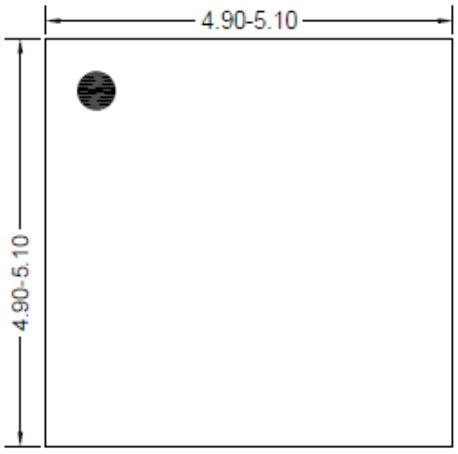


Fig.9 Design example VIN=37V-57V， PoE application, V_{out}=12V@1A

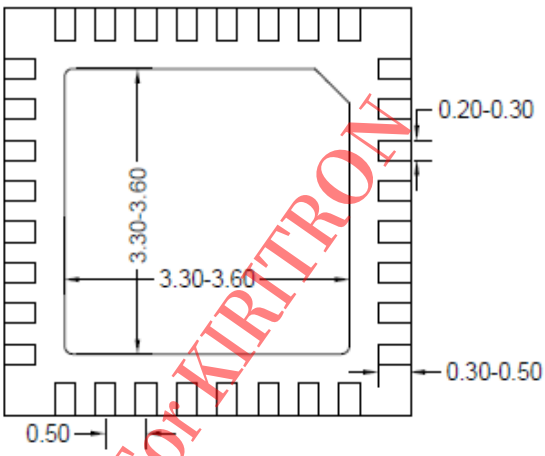
Silergy Corp.Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

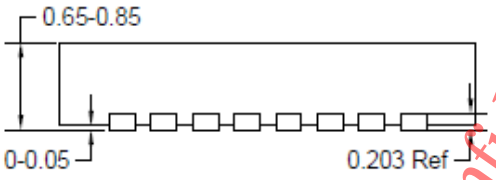
QFN5x5-32L Package outline & PCB Layout



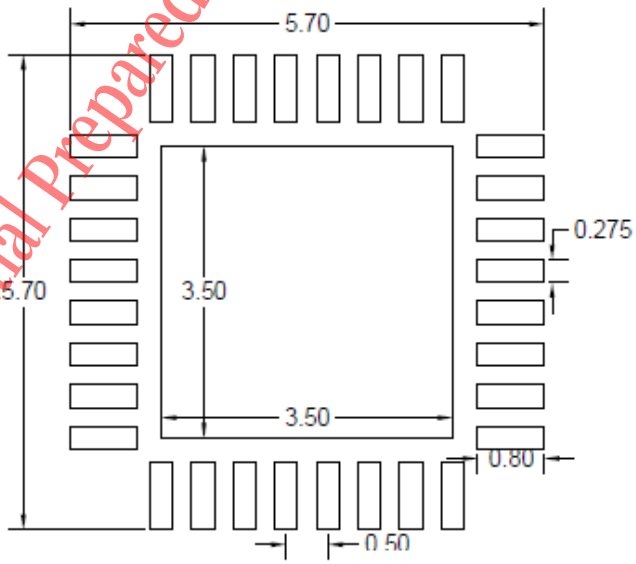
Top View



Bottom View



Side View



PCB layout (Recommended)

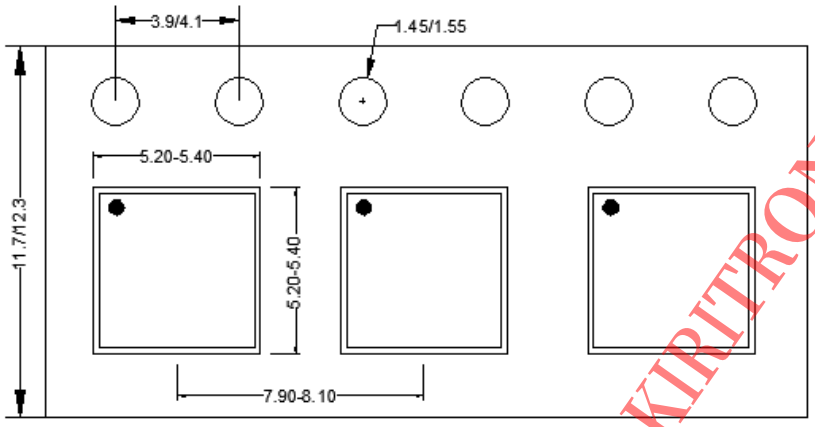
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Silergy Corp. Confidential Prepared For KIRTRON

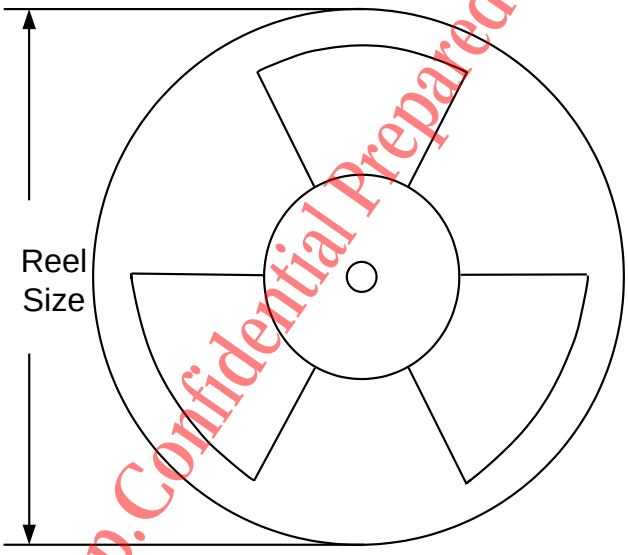
© 2022 Silergy Corp. All Rights Reserved.

Taping & Reel Specification

1. Taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
April 2, 2022	Revision 0.9B	Update the V_{VCC_SCP} Threshold
April 15, 2021	Revision 0.9A	Update the Package outline & PCB Layout information
October 23, 2020	Revision 0.9	Initial Release

Silergy Corp. Confidential Prepared For KIRITRON

© 2022 Silergy Corp. All Rights Reserved.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2022 Silergy Corp. **All Rights Reserved.**

Silergy Corp.Confidential Prepared For KIRUPO1

© 2022 Silergy Corp. All Rights Reserved.