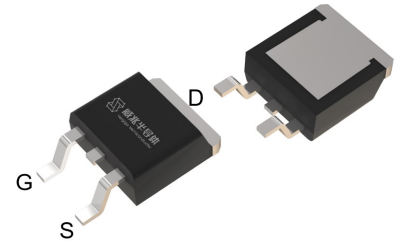


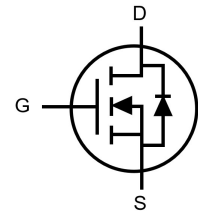
Features

- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® II Technology
- 100% Avalanche Tested, Rg 100% Tested

V_{DS}	100	V
$R_{DS(on),TYP@ V_{GS}=10V}$	3.6	mΩ
$I_D(\text{Wire bond limited})$	130	A


TO-263


Part ID	Package Type	Marking	Packing
VS1602GMH	TO-263	1602GMH	800pcs/Reel



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V
V_{GS}	Gate-Source voltage	±20	V
I_S	Diode continuous forward current (Wire bond limited)	$T_C = 25^\circ\text{C}$ 130	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Wire bond limited)	$T_C = 25^\circ\text{C}$ 130	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$ 120	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$ 675	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$ 16	A
		$T_A = 70^\circ\text{C}$ 12	A
E_{AS}	Maximum Avalanche energy, single pulsed ②	484	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$ 250	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$ 2.1	W
T_J, T_{STG}	Operating junction and storage temperature range	-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.5	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	50	60	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C) ^⑦	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.5	3	3.5	V
R _{DS(on)}	Drain-Source On-State Resistance ^⑧	V _{GS} =10V, I _D =40A	--	3.6	4.5	mΩ
		(T _j =100°C) ^⑦	--	4.7	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance ^⑦	V _{DS} =50V, V _{GS} =0V, f=100KHz	--	5195	--	pF
C _{oss}	Output Capacitance ^⑦		--	875	--	pF
C _{rss}	Reverse Transfer Capacitance ^⑦		--	30	--	pF
R _g	Gate Resistance	f=1MHz	--	1.8	--	Ω
Q _g	Total Gate Charge ^⑦	V _{DS} =50V, I _D =40A, V _{GS} =10V	--	91	--	nC
Q _{gs}	Gate-Source Charge ^⑦		--	25	--	nC
Q _{gd}	Gate-Drain Charge ^⑦		--	25	--	nC
Switching Characteristics ^⑦						
T _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	21	--	ns
T _r	Turn-on Rise Time		--	69	--	ns
T _{d(off)}	Turn-Off Delay Time		--	57	--	ns
T _f	Turn-Off Fall Time		--	70	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.8	1.2	V
T _{rr}	Reverse Recovery Time ^⑦	I _{sd} =40A, V _{GS} =0V	--	59	--	ns
Q _{rr}	Reverse Recovery Charge ^⑦	di/dt=100A/μs	--	71	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 44A, V_{GS} = 10V; 100% FT tested at L = 0.5mH, I_{AS} = 22A.
- ③ The power dissipation P_d is based on T_j(max), using junction-to-case thermal resistance R_{θJC}.
- ④ The power dissipation P_{dsm} is based on T_j(max), using junction-to-ambient thermal resistance R_{θJA}.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.
- ⑥ The value of R_{θJA} is measured with the device in a still air environment with T_A = 25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

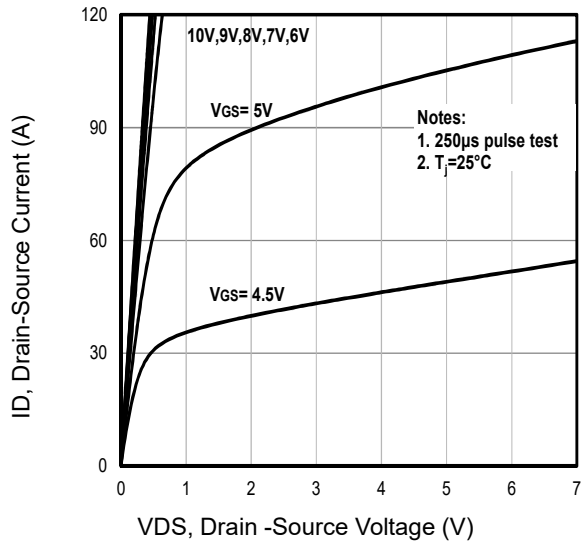


Fig1. Typical Output Characteristics

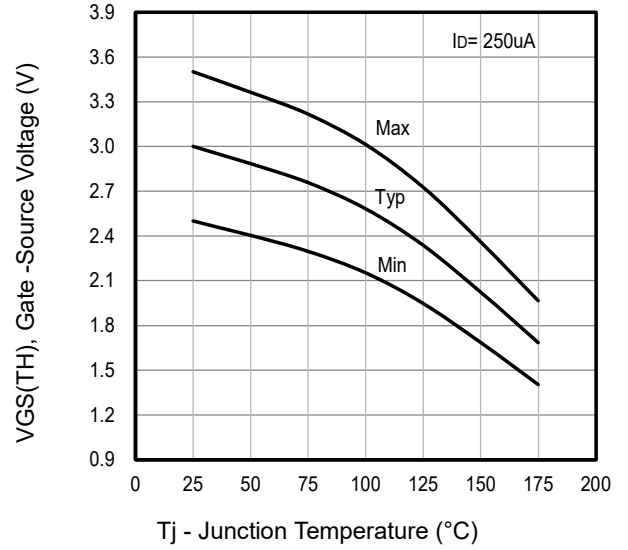


Fig2. VGS(TH) Gate-Source Voltage Vs. Tj

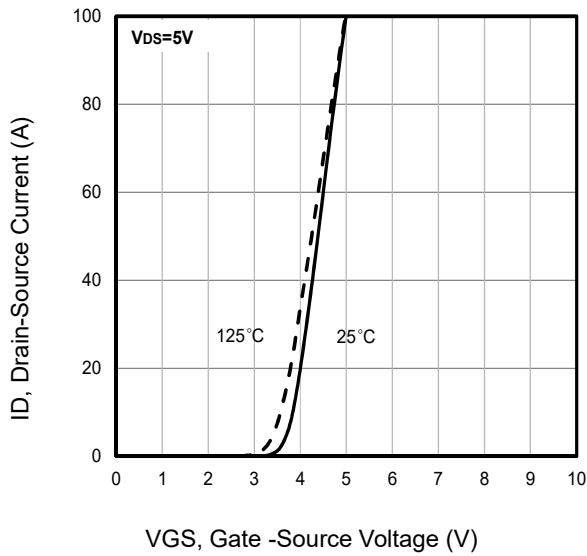


Fig3. Typical Transfer Characteristics

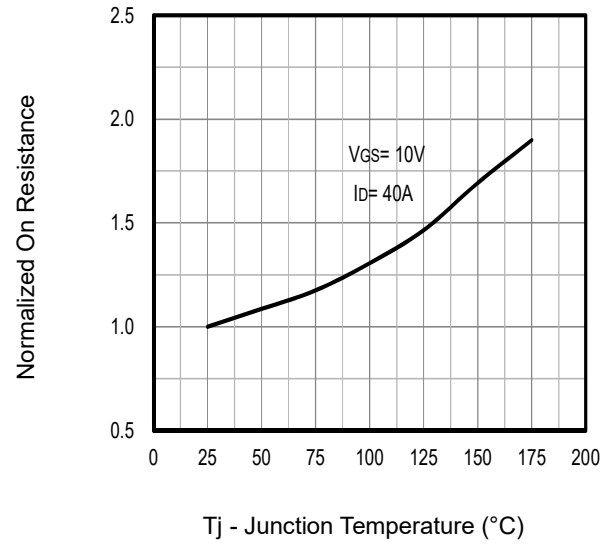


Fig4. Typical Normalized On-Resistance Vs. Tj

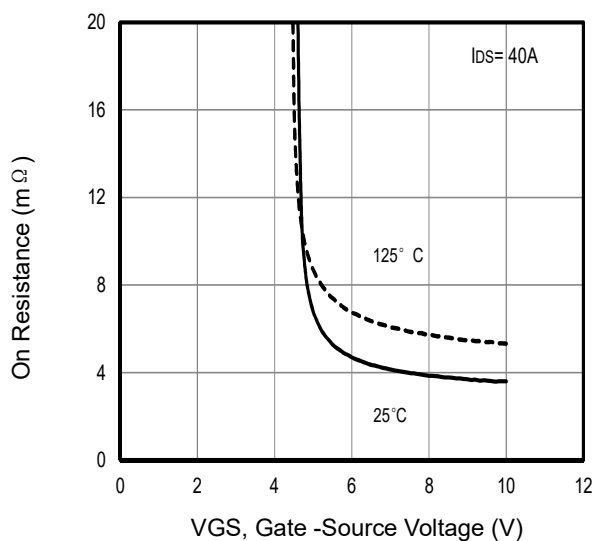


Fig5. Typical On Resistance Vs Gate-Source Voltage

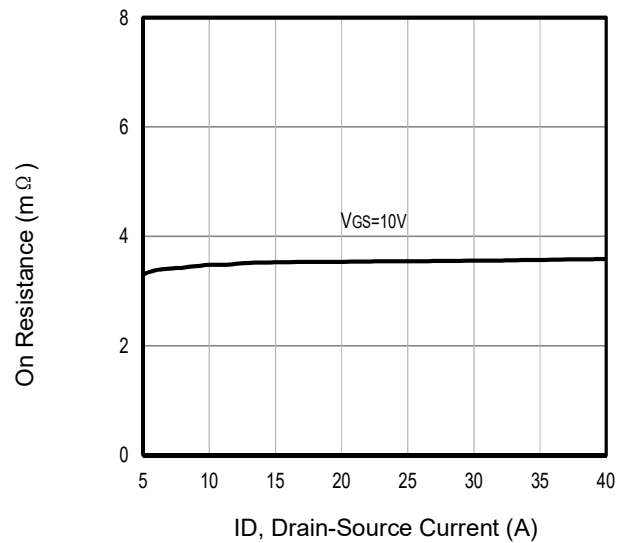


Fig6. Typical On Resistance Vs Drain Current and Gate

Typical Characteristics

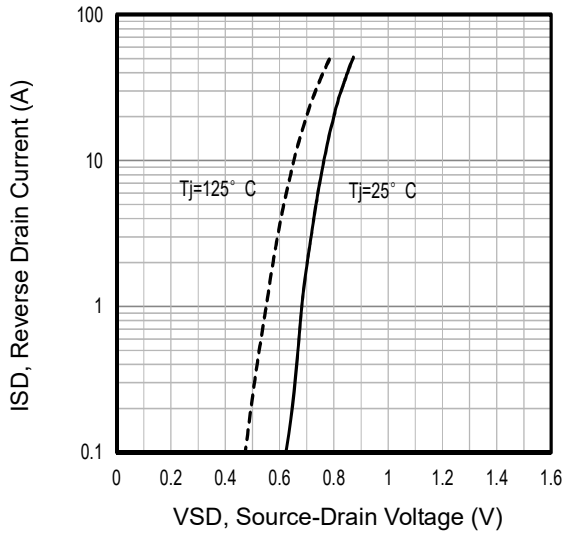


Fig7. Typical Source-Drain Diode Forward Voltage

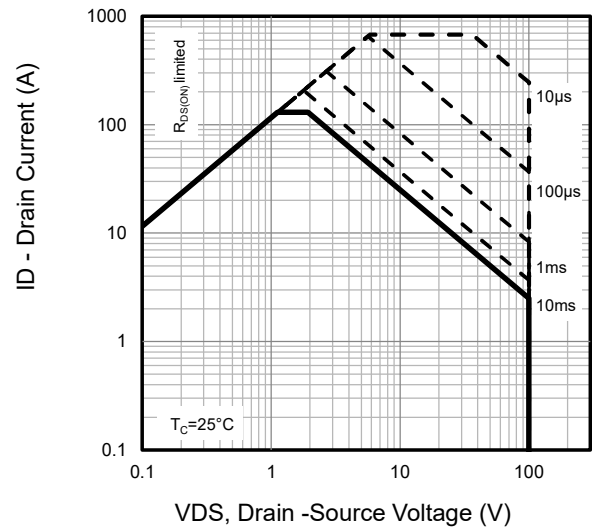


Fig8. Maximum Safe Operating Area

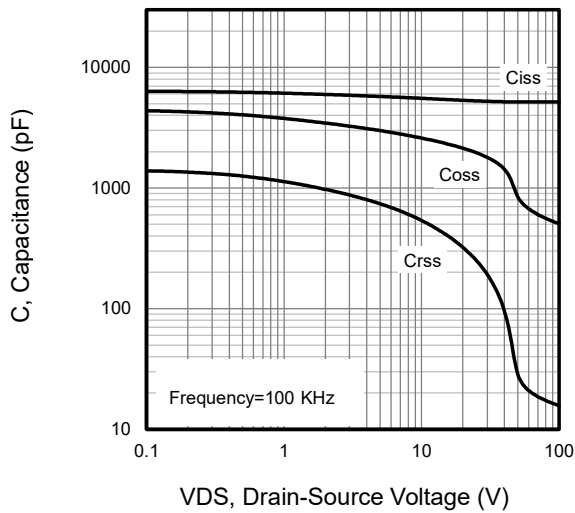


Fig9. Typical Capacitance Vs. Drain-Source Voltage

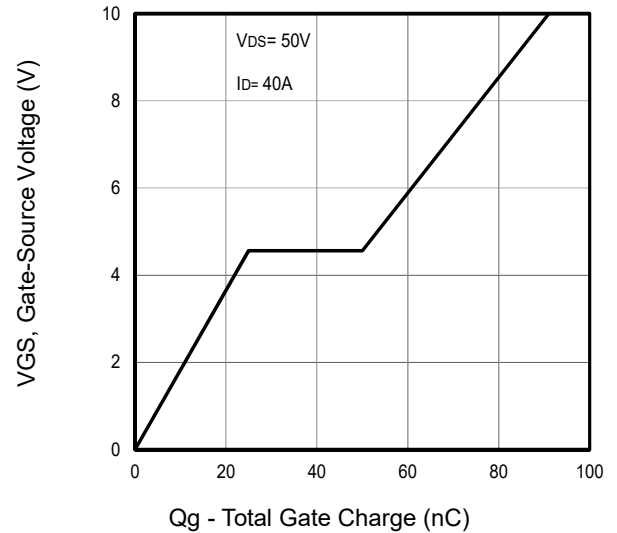


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

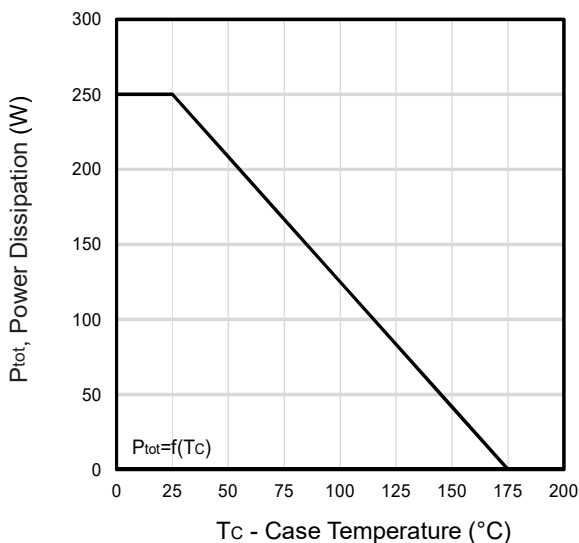


Fig11. Power Dissipation Vs. Case Temperature

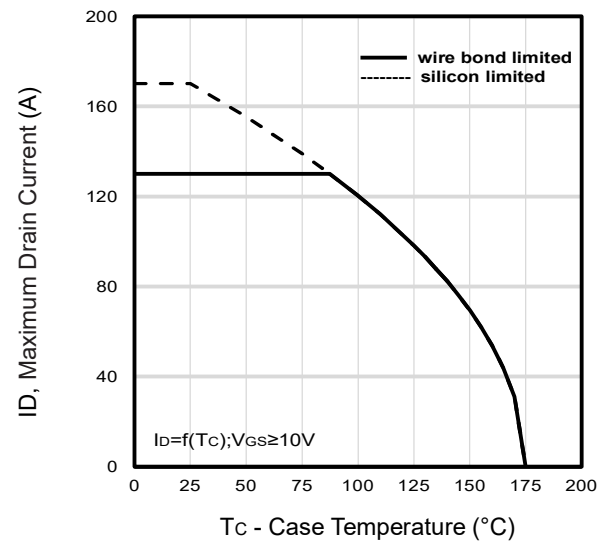


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

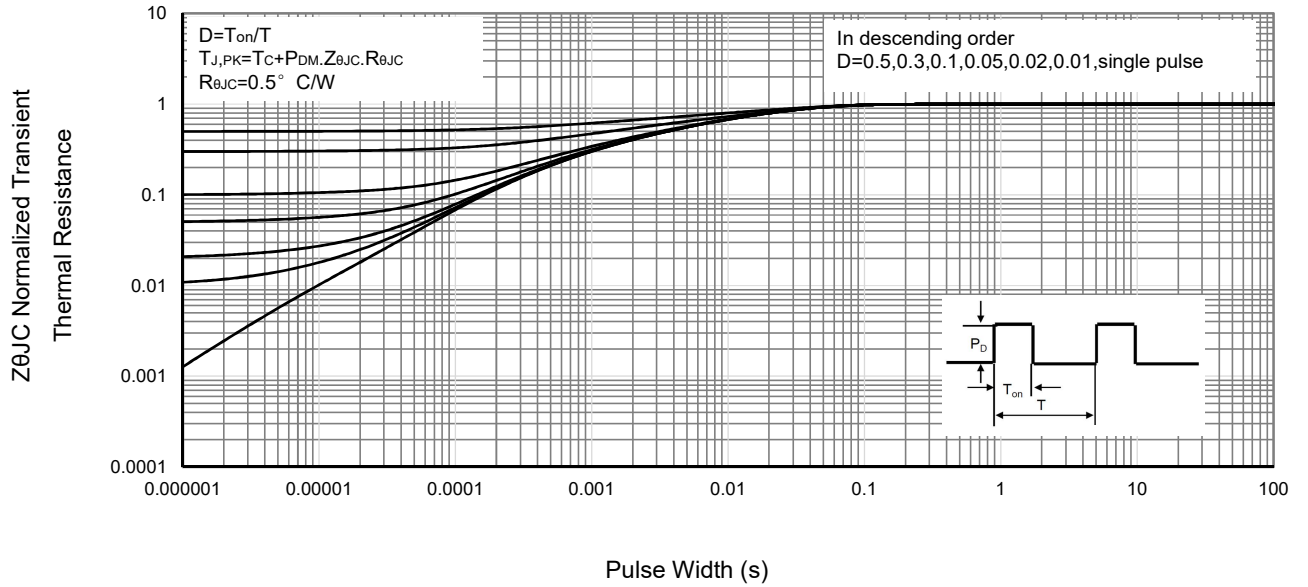


Fig13 . Normalized Maximum Transient Thermal Impedance

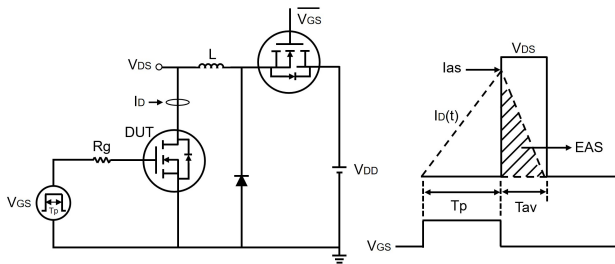


Fig14. Unclamped Inductive Test Circuit and waveforms

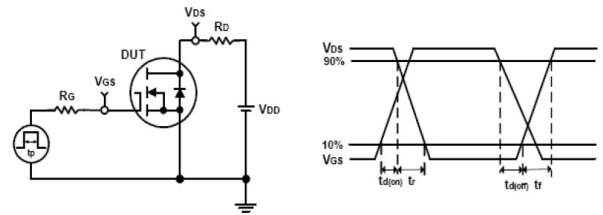
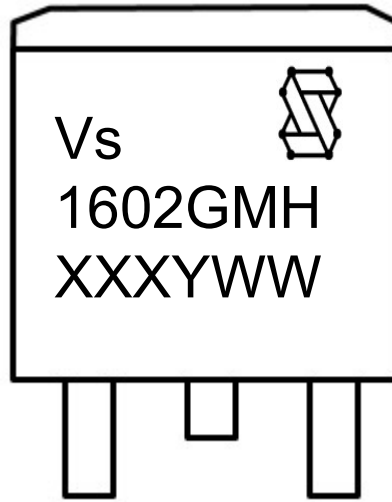


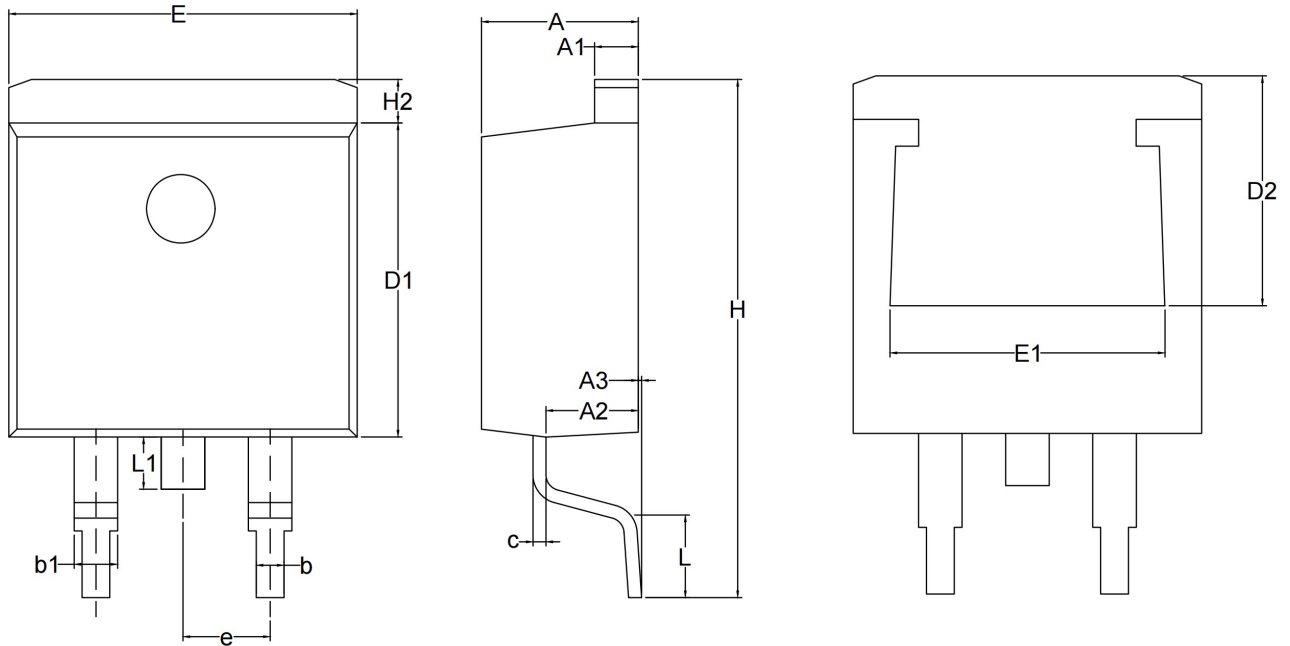
Fig15. Switching Time Test Circuit and waveforms

Marking Information



- 1st line: Vergiga Code (Vs), Vergiga Logo
- 2nd line: Part Number (1602GMH)
- 3rd line: Date code (XXXYWW)
 - XXX: Wafer Lot Number Code , code changed with Lot Number
 - Y: Year Code, refer to table below
 - WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-263 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.37	4.57	4.77
A1	1.22	1.27	1.42
A2	2.49	2.69	2.89
A3	0.00	0.13	0.25
b	0.70	0.81	0.96
b1	1.17	1.27	1.47
c	0.30	0.38	0.53
D1	8.50	8.70	8.90
D2	6.60	--	--
E	9.86	10.16	10.36
E1	7.06	--	--
e	2.54 BSC		
H	14.70	15.10	15.50
H2	1.07	1.27	1.47
L	2.00	2.30	2.60
L1	1.40	1.55	1.70

Notes:

1. Refer to JEDEC TO-263 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.