NSi83085x/NSi83086x

High Reliability Isolated Half and Full-Duplex RS-485 Transceivers

Datasheet (EN) 1.4

Product Overview

NSi83085x is a high reliability isolated half duplex RS-485 transceiver based on NOVOSENSE digital isolation technology, while NSi83086x is an isolated full duplex RS-485 transceiver. Both devices are safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption.

The Bus pins of NSi83085x/NSi83086x are protected from ±10kV system level ESD to GND2 on Bus side. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

The data rate of NSi83085x is 500kbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line. The data rate of NSi83086x is up to 16Mbps.

Key Features

- Up to 5000V$_{rms}$ Insulation voltage
- Bus side power supply voltage: 3.0V to 5.5V
- VDD1 supply voltage: 2.5V to 5.5V
- High CMTI: ±150kV/us
- High system level EMC performance:

  Bus Pins meet IEC61000-4-2 ±10kV ESD
- Fail-safe protection receiver
- Up to 256 transceivers on the bus
- Isolation Barrier Life: >60 years
- Operation temperature: -40℃~105℃
- RoHS-compliant packages:

  SOW16

Safety Regulatory Approvals

- UL recognition: up to 5000V$_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

Device Information

Part Number	*Package*	*Body Size*
NSI8308xA-DSWR	SOW16	10.30mm × 7.50mm
NSI8308x	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

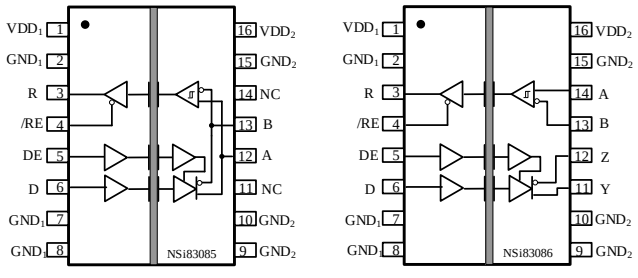

Figure 1. NSi83085x & NSi83086x Block Diagrams

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1. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD_1, VDD_2	-0.5		6	V	
Maximum Input Voltage	/RE, DE, TxD	-0.4		VDD+0.4	V	
Driver Output/Receiver Input Voltage	VA, VB, VY, VZ	-7		12	V	
Differential input voltage,A with repect to B	V_{ID}	-18		18	V	
Receiver Output Current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			4.62	kV	
Operating Temperature	Topr	-40		105	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM (Bus pins and GND)			±8000	V	
	HBM(All pins)			±6000	V	
	CDM			±2000	V	

2. Specifications

2.1. DC Electrical characteristics

(VDD1=2.5V~5.5V, VDD2=3.0V~5.5V, Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage	VDD_1	2.5		5.5	V	
	VDD_2	3.0		5.5	V	Bus Side
Logic-side supply current	I_{DD1}		2.97	4.98	mA	VDD_1=5V, DE=high, /RE=D =low, no load
			2.94	4.89	mA	VDD_1=3V, DE=high, /RE=D =low, no load
Bus-side supply current	I_{DD2}		2.83	5.02	mA	VDD_2=5V, DE=high, /RE=D =low, no load（NSi83085x）
			2.15	3.23	mA	VDD_2=5V, DE=high, /RE=D =low, no load（NSi83086x）
Thermal-Shutdown Threshold	T_{TS}		165		℃	

Thermal-Shutdown Hysteresis	T_{TSH}		15		℃	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	
Logic Side						
Input High Voltage	V_{IH}	2			V	DE, D, /RE
Input Low Voltage	V_{IL}			0.8	V	DE, D, /RE
Input Threshold	V_{IT}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS}		0.4		V	Input Threshold Hysteresis
Input Pull up Current	I_{PU}			20	uA	DE,/RE
Input Pull down Current	I_{PD}	-20			uA	DI
Output Voltage High	V_{OH}	VDD_1-0.3			V	I_{OH} = -4mA
Output Voltage Low	V_{OL}			0.3	V	I_{OL} = 4mA
Output Short-Circuit Current	I_{OSR}			150	mA	$0 \le V_R \le VDD_1$
Three-State Output Current	I_{OZ}	-15			uA	$0 \le V_R \le VDD_1$, /RE = high
Input Capacitance	C_{IN}		2		pF	DE, D, /RE
Driver						
Differential Output Voltage	$\lvert V_{OD} \rvert$			VDD2	V	No Load
		2.7		VDD2	V	See Figure 2.4.1, R_L=100Ω (RS-422),VDD2=5V
		1.5		VDD2	V	See Figure 2.4.1, R_L=100Ω (RS-422),VDD2=3.3V
		2.1		VDD2	V	See Figure 2.4.1, R_L=54Ω (RS-485),VDD2=5V
		1.3		VDD2	V	See Figure 2.4.1, R_L=54Ω (RS-485),VDD2=3.3V
Change in magnitude of the differential output voltage	$\Delta\lvert V_{OD} \rvert$			0.2	V	See Figure 2.4.1, R_L=100Ω or R_L=54Ω
Common-Mode Output Voltage	$\lvert V_{OC} \rvert$		$VDD_2/2$		V	See Figure 2.4.1, R_L=100Ω or R_L=54Ω
Change in Magnitude of Common-Mode Voltage	$\Delta\lvert V_{OC} \rvert$			0.2	V	See Figure 2.4.1, R_L=100Ω or R_L=54Ω
Driver Short-Circuit Output Current	I_{OSD}			250	mA	$0 \le V_{OUT} \le +12$ V
		-250			mA	$-7V \le V_{OUT} \le VDD_2$

Output Leakage Current (Y and Z) Full-Duplex	I_O			200	uA	DE=GND, VIN=12V
		-150			uA	DE=GND, VIN=-7V
Receiver						
Input Current (A and B)	I_A , I_B			200	uA	DE=GND, VDD_2=GND, V_{IN}=12V
		-150			uA	DE=GND, VDD_2=GND, V_{IN}=-7V
Receiver Differential Threshold Voltage	V_{TH}	-200	-125	-10	mV	$-7V \le V_{CM} \le 12V$
Receiver Input Hysteresis	ΔV_{TH}		15		mV	$V_A+V_B=0$
Receiver Input Resistance	R_{IN}	96			kΩ	$-7V \le V_{CM} \le 12V$, DE=low

2.2. switching Electrical characteristics

(VDD1=2.5V~5.5V, VDD2=3.0V~5.5V, Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Driver (NSi83085x)						
Maximum Data Rate	f_{MAX}	0.5			Mbps	
Driver Propagation Delay	t_{PLH}		24.4	60	ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
	t_{PHL}		24.2	60	ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
Driver Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		0.2		ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
Driver Output Falling Time or Rising time	t_F		14.4		ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
	t_R		14.4		ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
Driver Enable to Output High	t_{ZH}		20.4	60	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Driver Enable to Output Low	t_{ZL}		24.4	60	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Driver Output High to Disable	t_{HZ}		32.8	60	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Driver Output Low to Disable	t_{LZ}		28.6	60	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Receiver (NSi83085x)						

Maximum Data Rate	f_{MAX}	0.5			Mbps	
Receiver Propagation Delay	t_{PLH}		75	153	ns	See Figure 2.4.4， C_L=15pF
	t_{PHL}		74	138	ns	See Figure 2.4.4， C_L=15pF
Receiver Pulse Width Distortion	PWD		1		ns	$\lvert t_{PHL} - t_{PLH} \rvert$,See Figure 2.4.4， C_L=15pF
Receiver Output Falling Time or Rising time	t_F		2.5	5	ns	See Figure 2.4.4， C_L=15pF
	t_R		2.5	5	ns	See Figure 2.4.4， C_L=15pF
Receiver Enable to Output High	t_{ZH}		22	60	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF
Receiver Enable to Output Low	t_{ZL}		22	60	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF
Receiver Disable to Output High	t_{HZ}		23	60	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF
Receiver Disable to Output Low	t_{LZ}		23	60	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF
Driver (NSi83086x)						
Maximum Data Rate	f_{MAX}	16			Mbps	
Driver Propagation Delay	t_{PLH}		15.2	25	ns	See Figure 2.4.2， R_L=54Ω， C_L=50pF
	t_{PHL}		16.4	20.25	ns	See Figure 2.4.2， R_L=54Ω， C_L=50pF
Driver Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		1.2		ns	See Figure 2.4.2， R_L=54Ω， C_L=50pF
Driver Output Falling Time or Rising time	t_F		7.4	15	ns	See Figure 2.4.2， R_L=54Ω， C_L=50pF
	t_R		8.4	15	ns	See Figure 2.4.2， R_L=54Ω， C_L=50pF
Driver Enable to Output High	t_{ZH}		15.4	30	ns	See Figure 2.4.3， R_L=110Ω， C_L=50pF
Driver Enable to Output Low	t_{ZL}		15.4	30	ns	See Figure 2.4.3， R_L=110Ω， C_L=50pF
Driver Disable to Output High	t_{HZ}		28.2	50	ns	See Figure 2.4.3， R_L=110Ω， C_L=50pF
Driver Disable to Output Low	t_{LZ}		28.2	50	ns	See Figure 2.4.3， R_L=110Ω， C_L=50pF
Receiver (NSi83086x)						
Maximum Data Rate	f_{MAX}	16			Mbps	

Receiver Propagation Delay	t_{PLH}		65	100	ns	See Figure 2.4.4， C_L=15pF
	t_{PHL}		98	150	ns	See Figure 2.4.4， C_L=15pF
Receiver Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		33		ns	See Figure 2.4.4， C_L=15pF
Receiver Output Falling Time or Rising time	t_F		2.3	5	ns	See Figure 2.4.4， C_L=15pF
	t_R		2.1	5	ns	See Figure 2.4.4， C_L=15pF
Receiver Enable to Output High	t_{ZH}		12	20.7	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF
Receiver Enable to Output Low	t_{ZL}		13	18.9	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF
Receiver Disable to Output High	t_{HZ}		13.6	21	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF
Receiver Disable to Output Low	t_{LZ}		14	20.1	ns	See Figure 2.4.5， R_L=1kΩ， C_L=15pF

2.3. TYPICAL PERFORMANCE characteristics

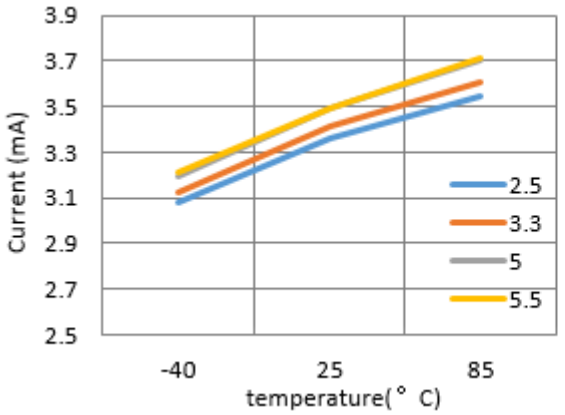


Figure 2.1 NSi83085x VDD1 supply current vs Temperature

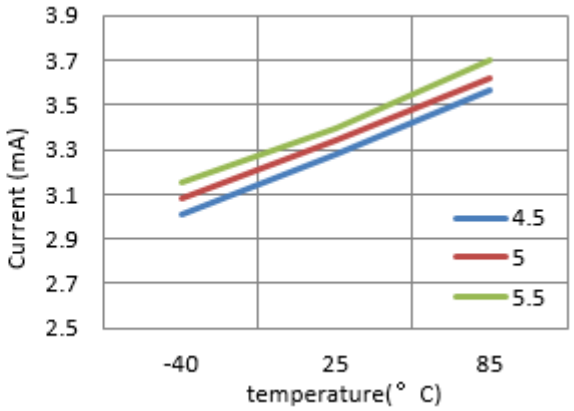
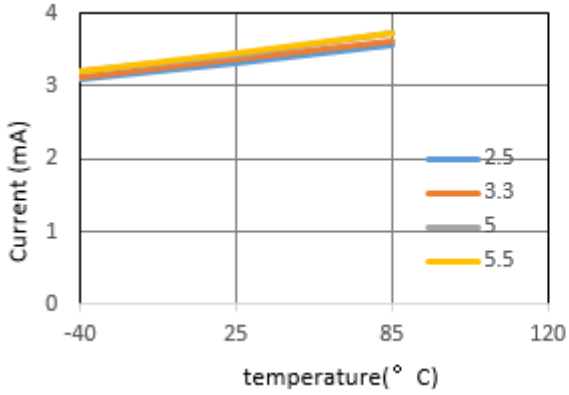


Figure 2.2 NSi83085x VDD2 supply current vs Temperature



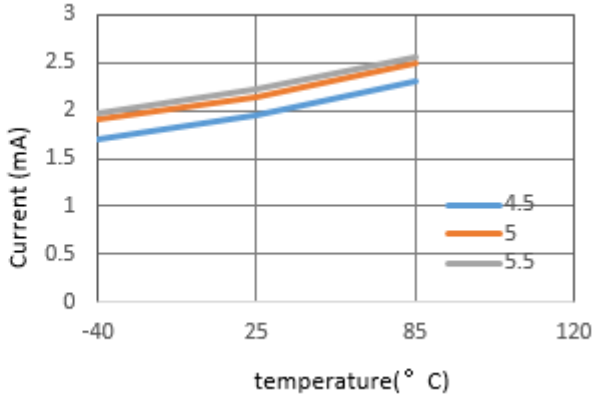


Figure 2.3 NSi83086x VDD1 supply current vs Temperature

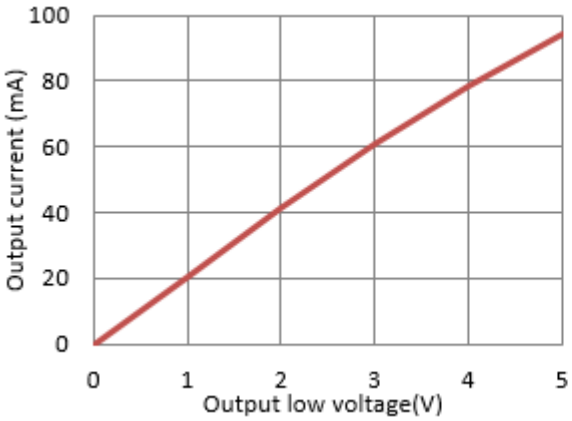


Figure 2.4 NSi83086x VDD2 supply current vs Temperature

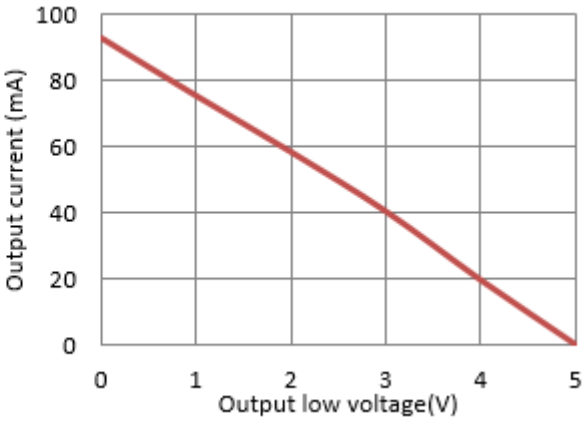
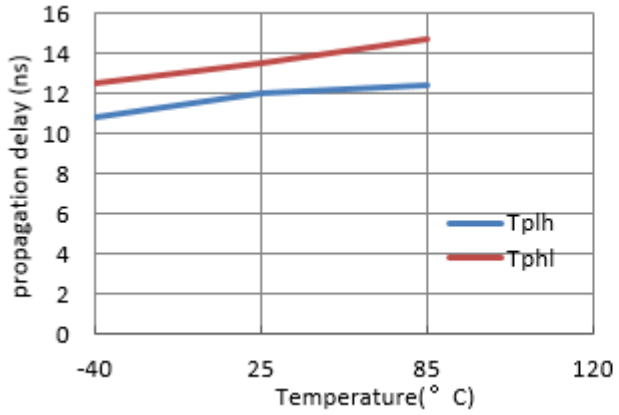


Figure 2.5 Receiver output current vs Output low voltage

Figure 2.6 Receiver output current vs Output High voltage



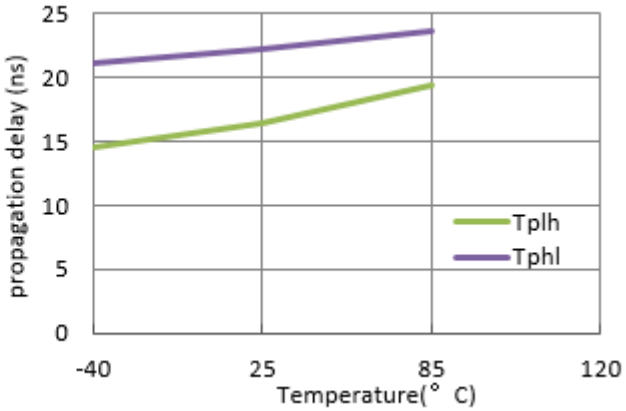
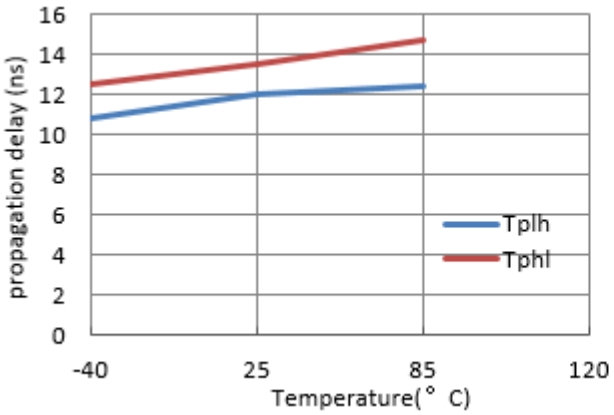


Figure 2.7 NSi83085x Transmitter Propagation Delay vs Temperature

Figure 2.8 NSi83085x Receiver Propagation Delay vs Temperature



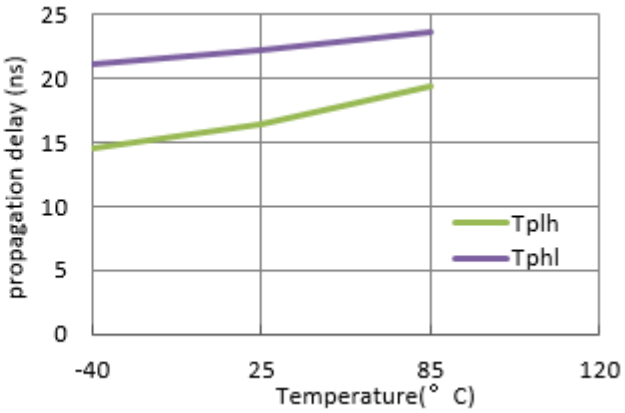


Figure 2.9 NSi83086x Transmitter Propagation Delay vs Temperature

Figure 2.10 NSi83086x Receiver Propagation Delay vs Temperature

2.4. Parameter Measurement Information

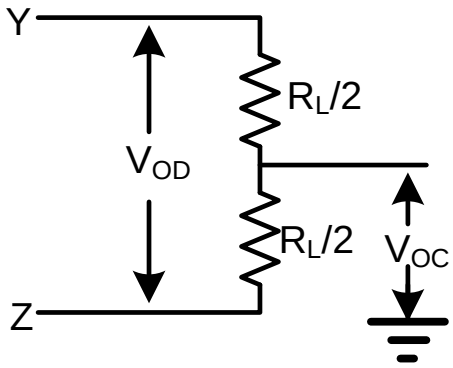


Figure 2.4.1 Driver DC Test Load

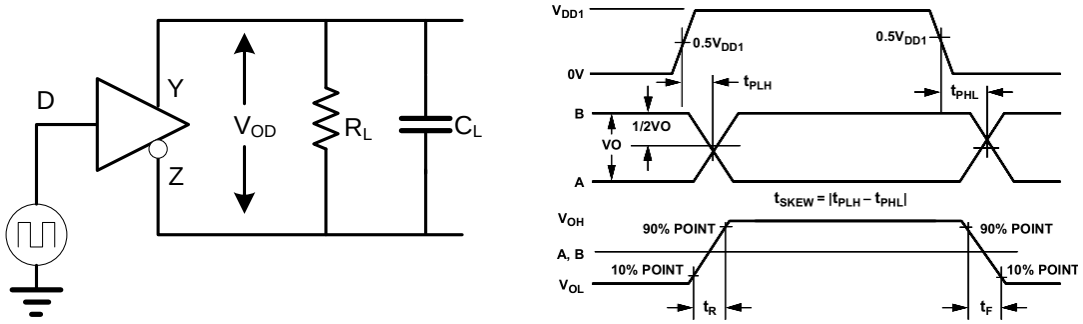


Figure 2.4.2 Driver Timing Test Circuit and waveform

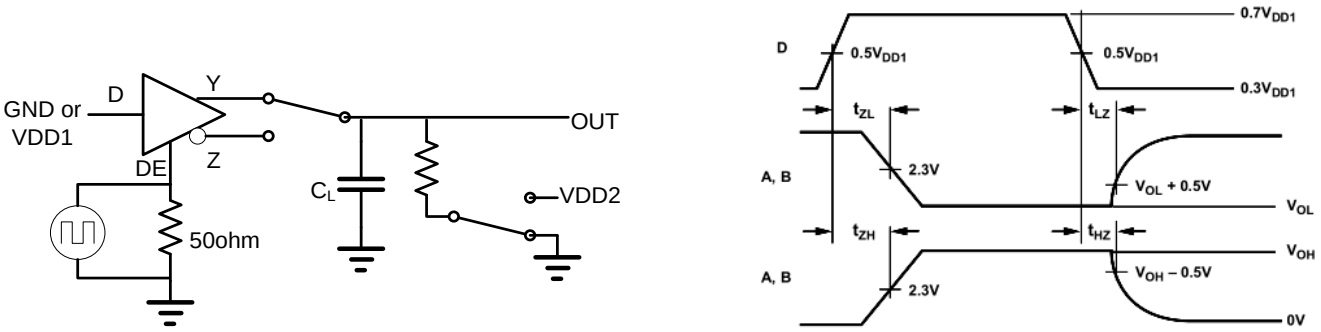


Figure 2.4.3 Driver Enable Disable Timing Test Circuit and waveform

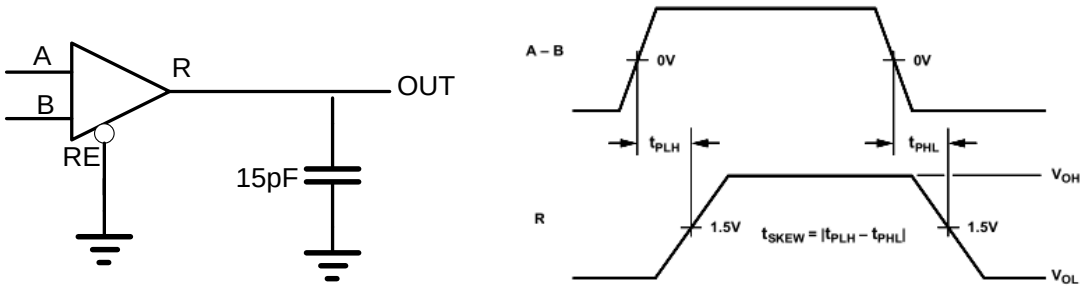


Figure 2.4.4 Receiver Propagation Delay Test Circuit and waveform

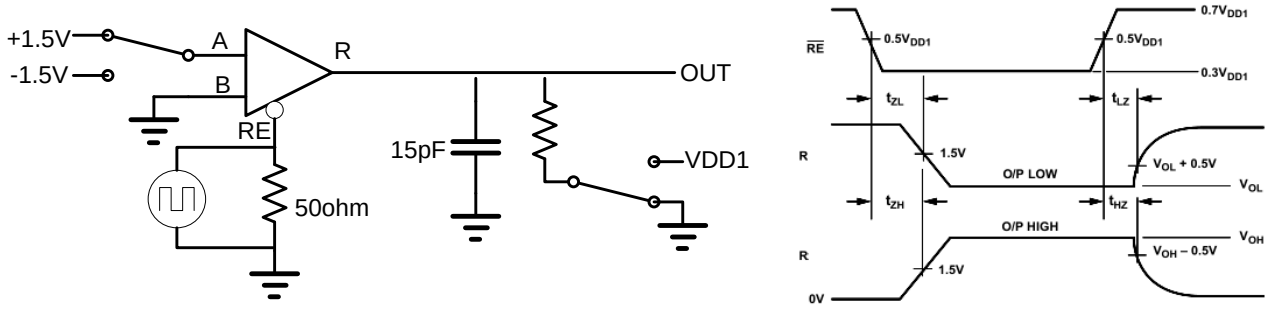


Figure 2.4.5 Receiver Enable Disable Timing Test Circuit and waveform

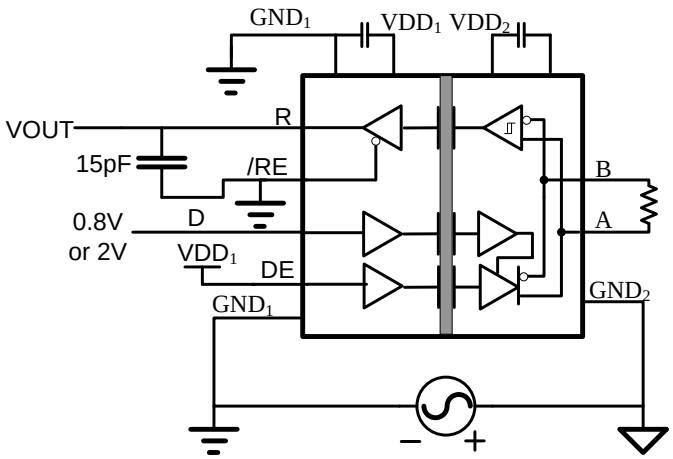


Figure 2.4.6 Common-Mode Transient Immunity Test Circuit

3. High Voltage Feature Description

3.1. insulation and safety related specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	L(I01)	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>600	**V**	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

3.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 insulation charateristics

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300Vrms			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 400Vrms			Ⅰ to Ⅳ	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage	AC Voltage(Bipolar)	V_{IORM}	1131	Vpeak
	AC Voltage(TDDB)	V_{IORM}	800	Vrms
	DC Voltage	V_{IORM}	1131	Vdc
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1749	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.3 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	Vpeak
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=1.3\times V_{IOSM}$	V_{IOSM}	5384	Vpeak
Isolation resistance	V_{IO} =500V	R_{IO}	$>10^9$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	pF
Input capacitance		C_I	2	pF
Total Power Dissipation at 25℃		Ps	1499	mW
	θ_{JA} = 84 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C		237	mA
Case Temperature		Ts	150	℃

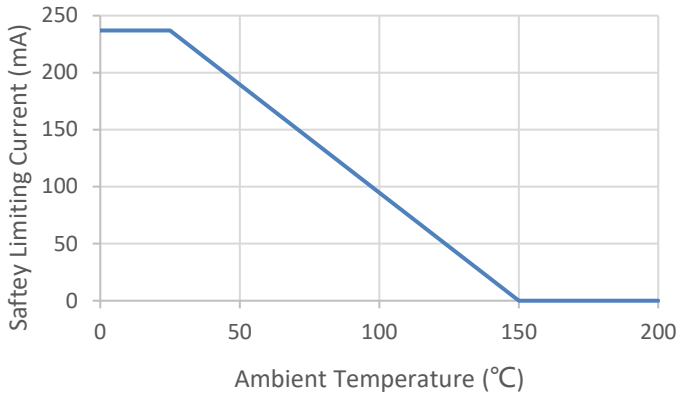


Figure 3.1 NSi83085x/NSi83086x Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

3.3. Regulatory information

The NSi83085x/NSi83086x are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000Vrms Isolation voltage	Single Protection, 5000Vrms Isolation voltage	Basic Insulation 1131Vpeak, V_{IOSM}=4615Vpeak	Basic insulation
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

[1] In accordance with UL 1577, each NSi83085x/NSi83086x is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

[2] In accordance with DIN VDE V 0884-11, each NSi8100W/NSi8101W is proof tested by applying an insulation test voltage ≥ 1273 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

4. Function Description

NSi83085x is a high reliability isolated half duplex RS-485 transceiver , while NSi83086x is an isolated full duplex RS-485 transceiver. Data isolation is achieved using Novosense integrated capacitive isolation that allows data transmission between the logic side and the Bus side. Both devices are safety certified by UL1577 support 5kV_{RMS} insulation withstand voltages.

4.1. Data rate

The data rate of NSi83085x is 500kbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line. The data rate of NSi83086x is up to 16Mbps.

4.2. True Fail-safe receiver inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -50mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage (V_A-V_B) is greater than or equal to -50mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

4.3. Truth tables

Table 4.1 Driver Function Table

VDD1 status	*VDD2 status*	*Input*	*Enable Input*	*Outputs[1]*

		(D)	*(DE)*	*A/Y*	*B/Z*
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

[1] PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance; Driver output pins are Y and Z for NSi83086x, A and B for NSi83085x;

Table 4.2 Reciever Function Table[1]

VDD1 status	*VDD2 status*	*Differential Input (V_A-V_B)*	*Enable Input (/RE)*	*Output (R)*
PU	PU	≥-50mV	L/Open	H
PU	PU	≤-200mV	L/Open	L
PU	PU	Open/Short	L/Open	H
PU	PU	X	H	Z
PU	PU	Idle	L	H
PD	PU	X	X	Z
PU	PD	X	X	H
PD	PD	X	X	Z

[1] PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

4.4. Thermal shutdown

The device is protected from over temperature damage by integrated thermal shutdown circuitry. When the junction temperature (TJ) exceeds +165°C (typ), the driver outputs go high-impedance. The device resumes normal operation when TJ falls below +145°C (typ).

5. Application Note

5.1. 256 transceivers on the bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

5.2. ESD protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handing and assembly. The Bus pins have extra protection against static electricity to both the logic side (VDD1 side) and bus side (VDD2 side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ± 8kV HBM.
- ±10kV using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±6kV HBM.
- ±7kV using the Contact Discharge method specified in IEC 61000-4-2

5.3. Layout considerations

The NSi83085x/NSi83086x requires a 0.1 µF bypass capacitor between VDD and GND. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B, Y and Z pins.

5.4. Typical application

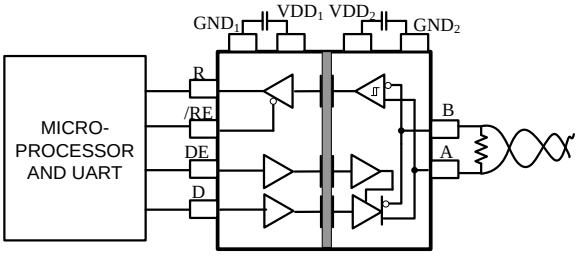


Figure 5.1 NSi83085x typical application circuit

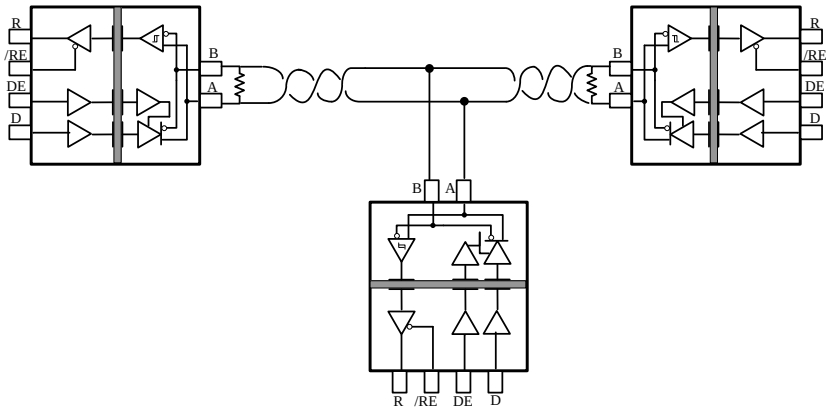


Figure 5.2 Typical isolated Half-Duplex RS-485 application

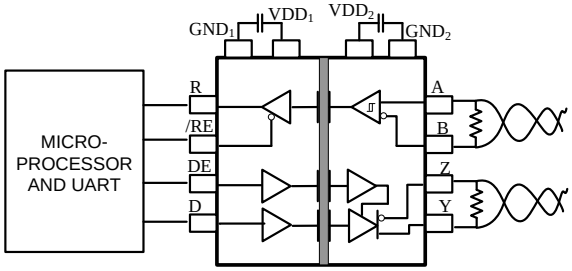


Figure 5.3 NSi83086x typical application circuit

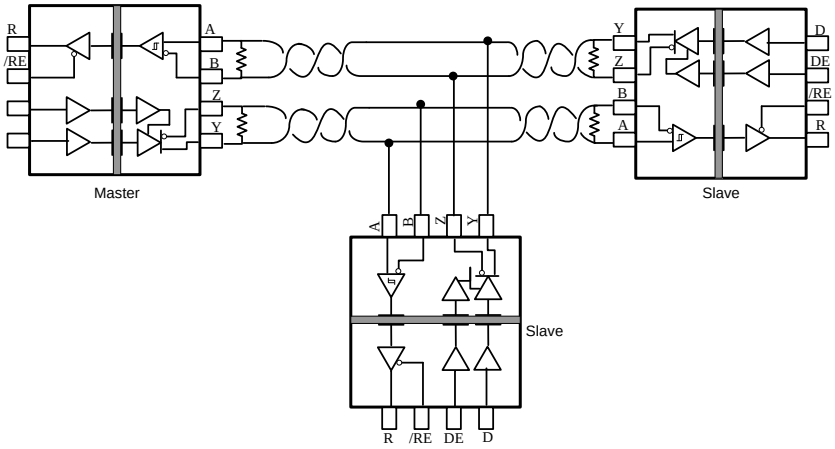


Figure 5.4 Typical isolated Full-Duplex RS-485 application

6. Package Information

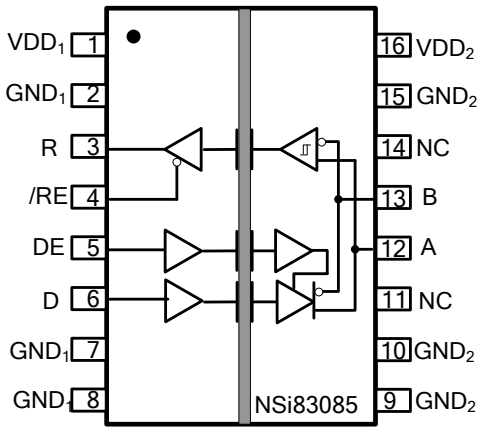


Figure 6.1 NSi83085x Package

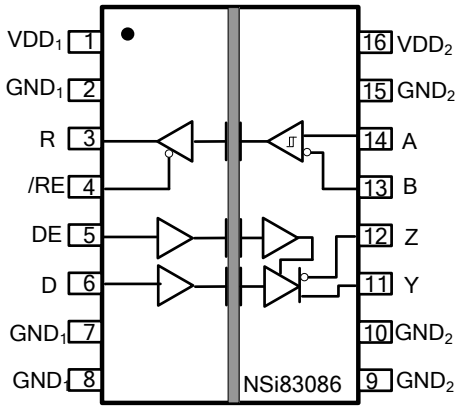
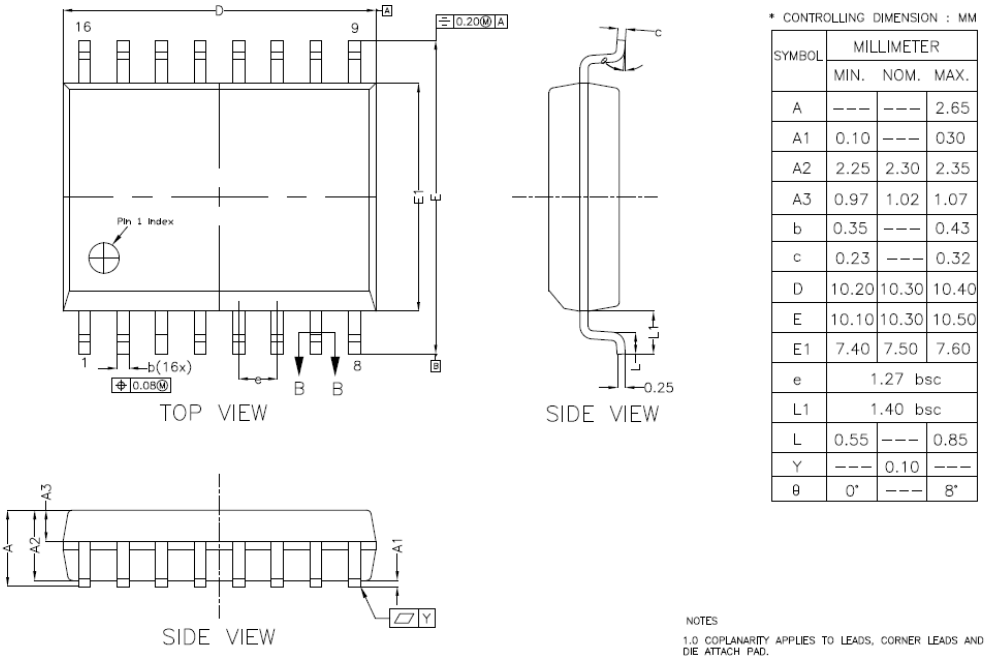


Figure 6.2 NSi83086x Package



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 6.3 SOIC16 Package Shape and Dimension in millimeters and (inches)

Table6.1 NSi83085x Pin Configuration and Description

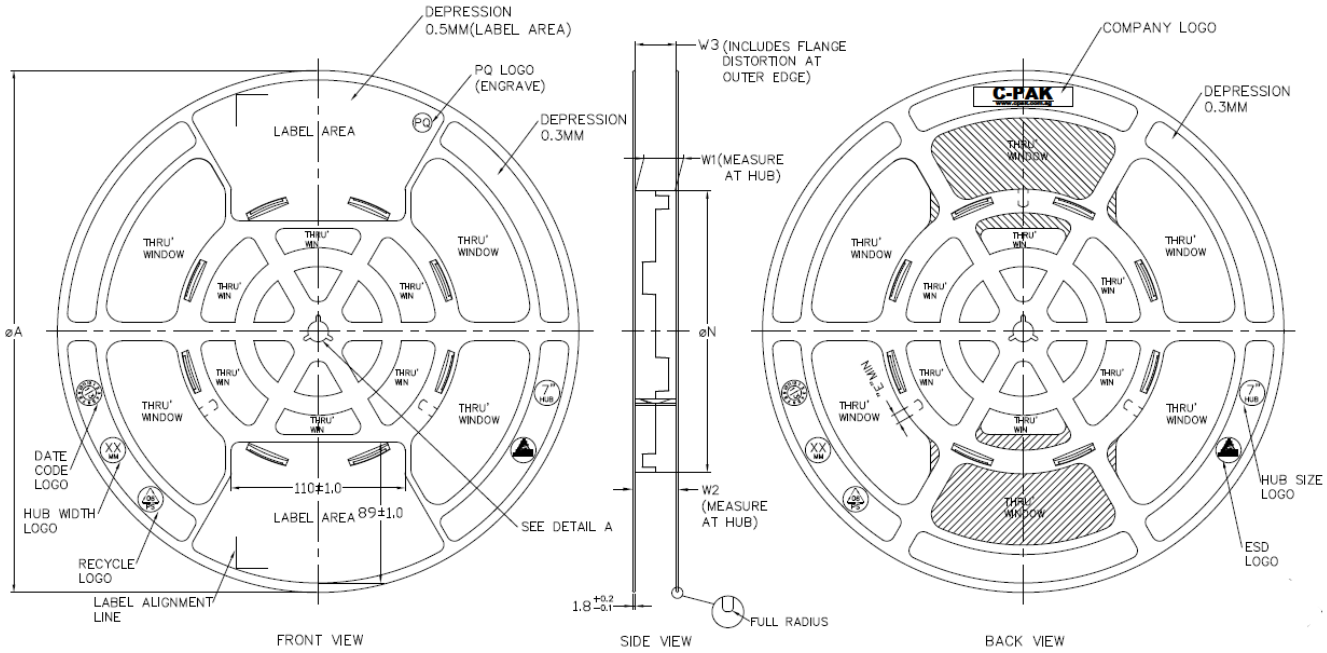
NSi83085x PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Isolator Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	R	Receive output
4	/RE	Receive enable input. This is an active low input.
5	DE	Driver enable input. This is an active high input
6	D	Driver transmit data input.
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	GND_2	Ground 2, the ground reference for Isolator Side 2
11	NC	No Connection.
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when VDD_1 or VDD_2 is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD_1 or VDD_2 is powered down, Pin B is put into a high impedance state to avoid overloading the bus.

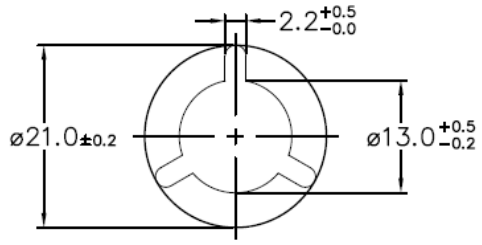
14	NC	No Connection.
15	GND_2	Ground 2, the ground reference for Isolator Side 2
16	VDD_2	Power Supply for Isolator Side 2

Table6.2 NSi83086x Pin Configuration and Description

NSi83086x PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Isolator Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	R	Receive output
4	/RE	Receive enable input. This is an active low input.
5	DE	Driver enable input. This is an active high input
6	D	Driver transmit data input.
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	GND_2	Ground 2, the ground reference for Isolator Side 2
11	Y	Noninverting Driver Output. When the driver is disabled, or when VDD_1 or VDD_2 is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
12	Z	Inverting Driver Output. When the driver is disabled, or when VDD_1 or VDD_2 is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Receiver Input.
14	A	Noninverting Receiver Input.
15	GND_2	Ground 2, the ground reference for Isolator Side 2
16	VDD_2	Power Supply for Isolator Side 2

7. Tape and Reel Information

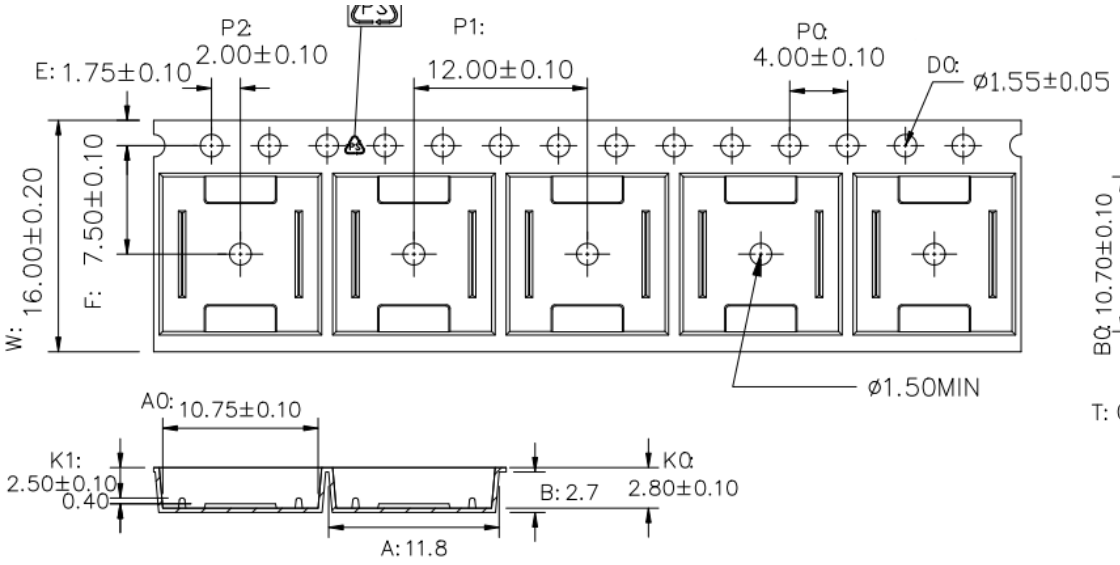




ARBOR HOLE
DETAIL A
SCALE : 3:1

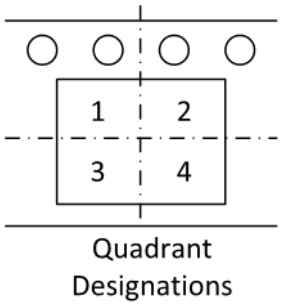
PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122）
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :10^{5} ~ 10^{10}Ω/□

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10



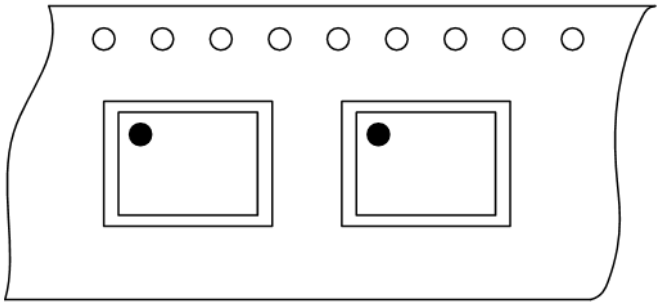


Figure 7.1 Tape and Reel Information of SOW16

8. Order Information

Part No.	*Isolation Rating(kV_{RMS})*	*Duplex*	*Max Data Rate (Mbps)*	*MSL*	*Temperature*	*No. of Nodes*	*Package*	*SPQ*
NSi83085A-DSWR	5	Half	0.5	3	-40 to 105℃	256	SOW16	1000
NSi83086A-DSWR	5	Full	16	3	-40 to 105℃	256	SOW16	1000
NSi83085	5	Half	0.5	3	-40 to 105℃	256	SOW16	1000
NSi83086	5	Full	16	3	-40 to 105℃	256	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.								

9. Revision History

Revision	Description	Date
1.0	Initial version	2020/12/5
1.1	Update format	2021/2/25
1.2	Added MSL information	2021/3/2
1.3	Added NSi83085 and NSi83086 information	2021/4/8
1.4	Correction MSL level	2021/6/8