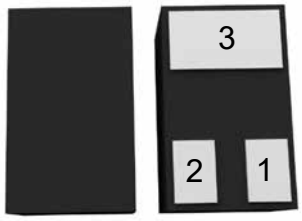
2N7002KN

N-Channel Enhancement Mode Power MOSFET



1. Gate 2.Source 3.Drain

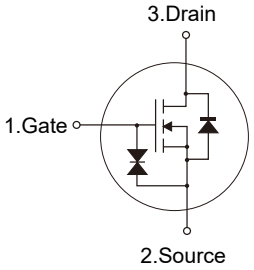
Simplified outline(DFN1006-3L)

Features

- Fast switching
- Low gate charge and $R_{DS(ON)}$
- Low reverse transfer capacitances
- V_{DS}= 60V ， I_D= 0.3A
  $R_{DS(ON)}$ < 3Ω @V_{GS}=10V
- ESD protected(HBM) up to 2KV

Application

- Load switch and in PWM applications
- Power management



Marking

Device	Marking	Shipping
2N7002KN	K72	10,000PCS/Reel&Tape

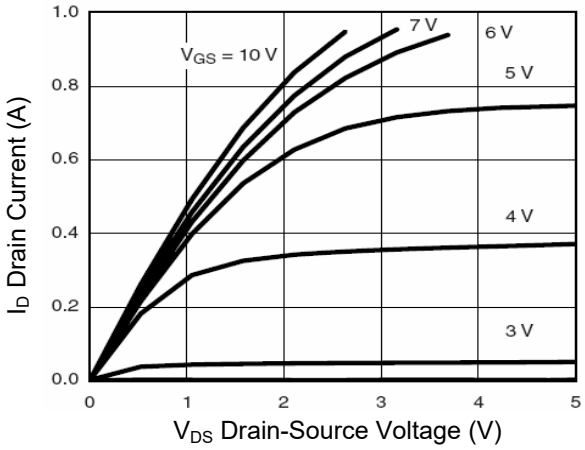
Absolute Maximum Ratings Ta = 25℃

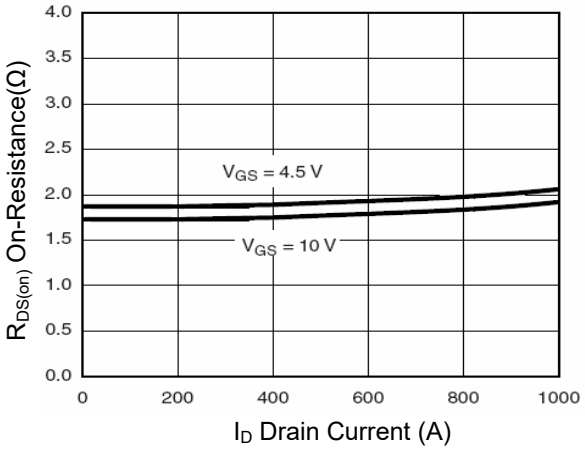
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	0.3	A
Drain Current-Pulsed Note1	I_{DM}	0.8	A
Maximum Power Dissipation	P_D	0.3	W
Operating Junction and Storage Temperature Range	$_J$,T_{STG}	150,-55~150	℃
Thermal Resistance,Junction-to-Ambient Note2	$R_{\theta JA}$	357	℃/W

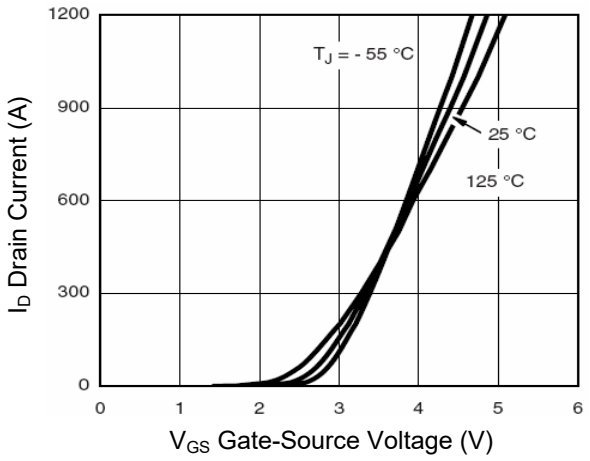
■ Electrical Characteristics Ta = 25℃

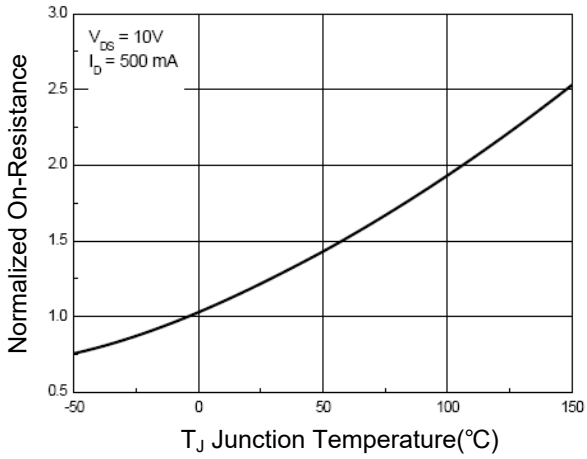
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	--	--	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	--	--	±10	μA
Gate Threshold Voltage Note3	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	1.4	2.5	V
Drain-Source On-Resistance Note3	$R_{DS(on)}$	V_{GS}=10V,I_D=0.5A	--	1.9	3	Ω
		V_{GS}=4.5V,I_D=0.3A	--	2.2	4	Ω
Forward Transconductance Note3	g_{FS}	V_{DS}=10V,I_D=0.2A	0.1	--	--	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHz	--	21	--	pF
Output Capacitance	C_{oss}		--	11	--	pF
Reverse Transfer Capacitance	C_{rss}		--	4.2	--	pF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=30V,V_{GEN}=10V, I_D=0.2A,R_G=10Ω	--	10	--	ns
Turn-on Rise Time	t_r		--	50	--	ns
Turn-off Delay Time	$t_{d(off)}$		--	17	--	ns
Turn-off Fall Time	t_f		--	10	--	ns
Total Gate Charge	Q_g	V_{DS}=10V,V_{GS}=4.5V,I_D=0.3A	--	1.7	--	nC
Source-Drain Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=0.2A	--	--	1.2	V
Diode Forward Current	I_S		--	--	0.3	A

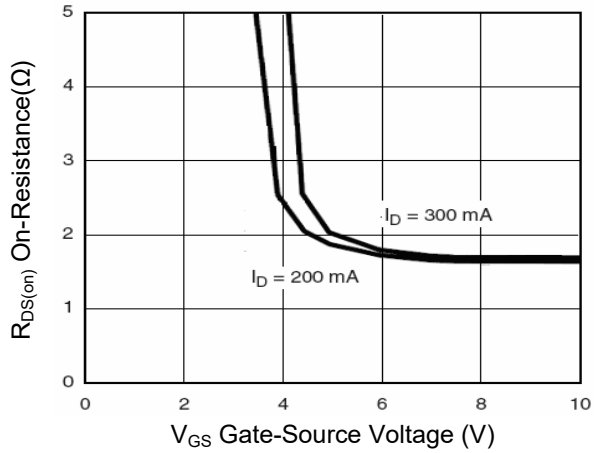
Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse width≤300μs, duty cycle≤2%.

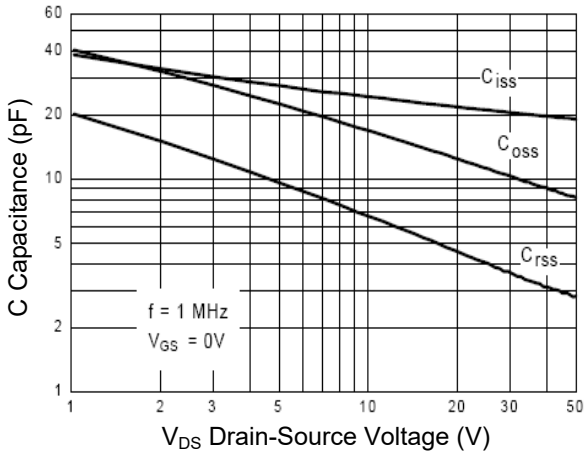

1.0
0.8
0.6
0.4
0.2
0.0
0
1
2
3
4
5
VGS = 10 V
7 V
6 V
5 V
4 V
3 V
ID Drain Current (A)
VDS Drain-Source Voltage (V)

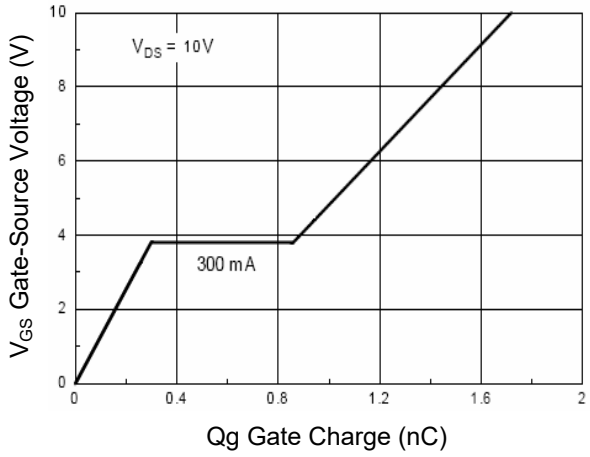

4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
200
400
600
800
1000
VGS = 4.5 V
VGS = 10 V
RDS(on) On-Resistance(Ω)
ID Drain Current (A)

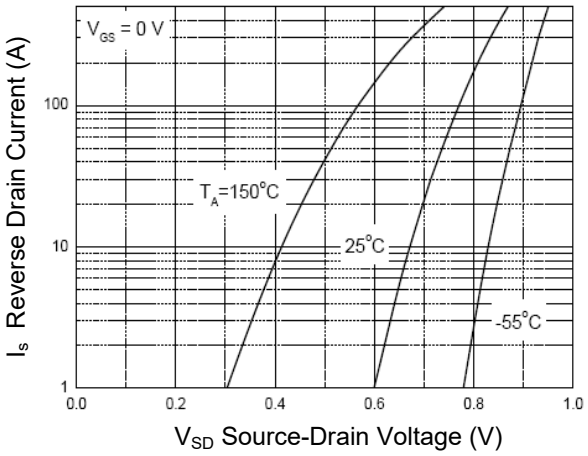

1200
900
600
300
0
0
1
2
3
4
5
6
TJ = - 55 °C
25 °C
125 °C
ID Drain Current (A)
VGS Gate-Source Voltage (V)

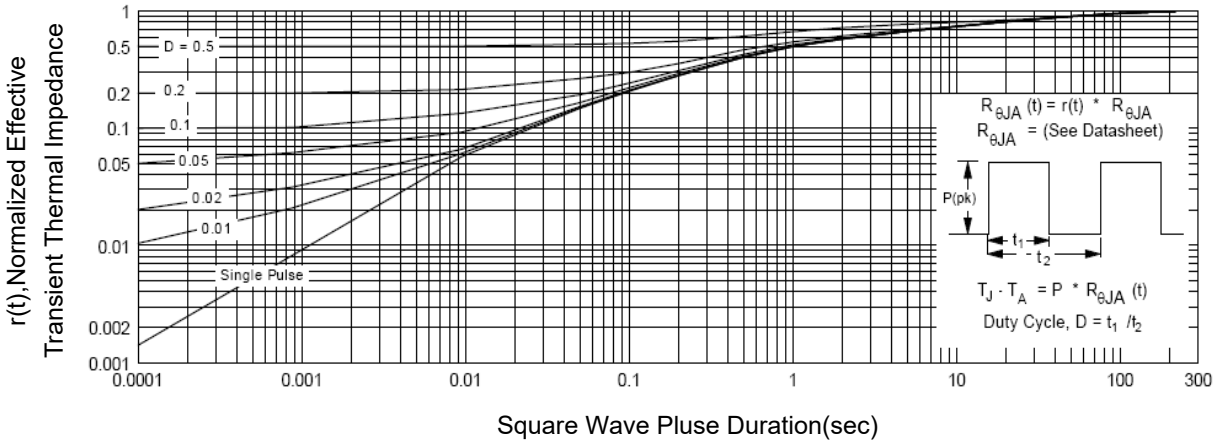

3.0
2.5
2.0
1.5
1.0
0.5
-50
0
50
100
150
VDS = 10V
ID = 500 mA
Normalized On-Resistance
TJ Junction Temperature(°C)


5
4
3
2
1
0
0
2
4
6
8
10
ID = 300 mA
ID = 200 mA
RDS(on) On-Resistance(Ω)
VGS Gate-Source Voltage (V)


60
40
20
10
5
2
1
1
2
3
5
10
20
30
50
Ciss
Coss
Crss
f = 1 MHz
VGS = 0V
C Capacitance (pF)
VDS Drain-Source Voltage (V)


V_{DS} = 10V
300 mA
V_{GS} Gate-Source Voltage (V)
Qg Gate Charge (nC)


V_{GS} = 0 V
T_A=150°C
25°C
-55°C
I_S Reverse Drain Current (A)
V_{SD} Source-Drain Voltage (V)


D = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
$R_{\theta JA}(t) = r(t) * R_{\theta JA}$
$R_{\theta JA}$ = (See Datasheet)
P(pk)
t_1
t_2
$T_J - T_A = P * R_{\theta JA}(t)$
Duty Cycle, D = t_1 /t_2
r(t),Normalized Effective Transient Thermal Impedance
Square Wave Pluse Duration(sec)

■ **DFN1006-3L**

Dimensions in mm