ME2324D/ME2324D-G

N-Channel 25V (D-S) MOSFET, ESD Protected

GENERAL DESCRIPTION

The ME2324D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 400m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 450m\Omega @ V_{GS}=2.7V$
- ESD Protection HBM >1KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

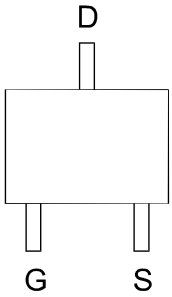
APPLICATIONS

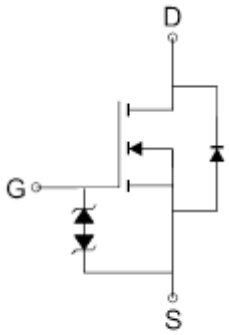
- Power Management in Note book
- Portable Equipment
- Load Switch

PIN CONFIGURATION

(SOT-23)

Top View





N-Channel

Ordering Information: ME2324D(Pb-free)

ME2324D-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	0.71	A
	T_A=70℃		0.57	
Pulsed Drain Current		I_{DM}	2.8	A
Maximum Power Dissipation	T_A=25℃	P_D	0.35	W
	T_A=70℃		0.22	
Junction and Storage Temperature Range		T_J ,Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	357	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	25			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.5		1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=25V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=4.5V, I_D= 0.4A		300	400	mΩ
		V_{GS}=2.7V, I_D= 0.2A		340	450	
V_{SD}	Diode Forward Voltage	I_S=0.29A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=5V, V_{GS}=10V, I_D=0.2A		5.8		nC
Qg	Total Gate Charge	V_{DS}=5V, V_{GS}=4.5V, I_D=0.2A		2.6		
Qgs	Gate-Source Charge			1.8		
Qgd	Gate-Drain Charge			0.3		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHZ		90		pf
Coss	Output Capacitance			26		
Crss	Reverse Transfer Capacitance			7		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=6V, R_L =12Ω I_D=0.2A, V_{GEN}=4.5V R_G=50Ω		13		ns
t_r	Turn-On Rise Time			6		
$t_{d(off)}$	Turn-Off Delay Time			54		
t_f	Turn-Off Fall Time			11		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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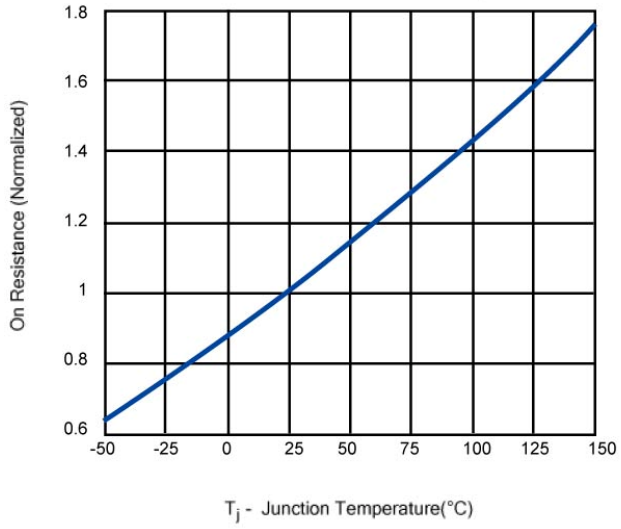
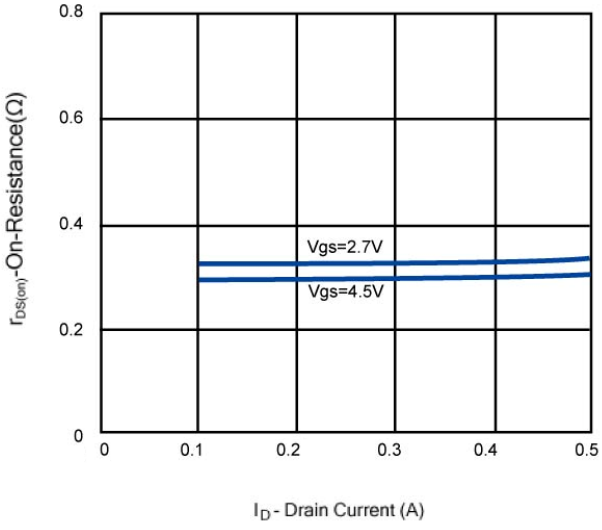
Typical Characteristics (T_J =25℃ Noted)

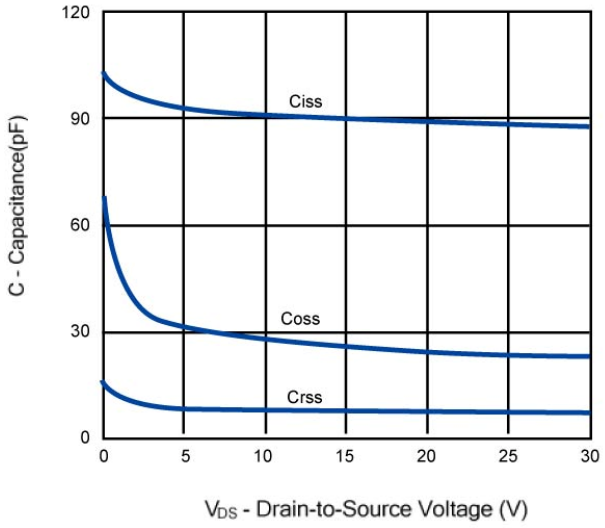
On Resistance vs. Junction Temperature



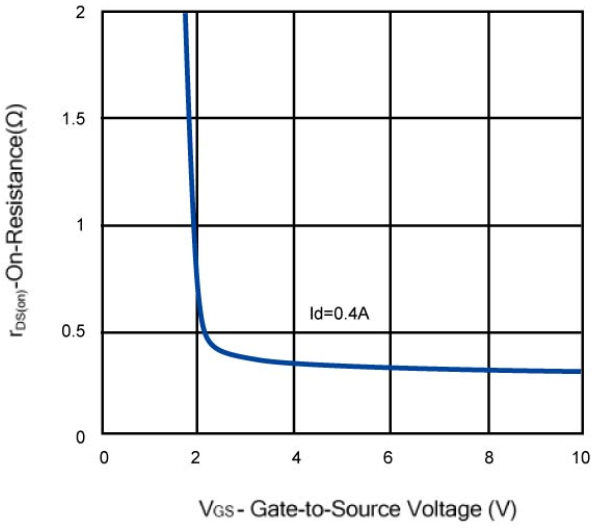
On-Resistance vs. Drain Current



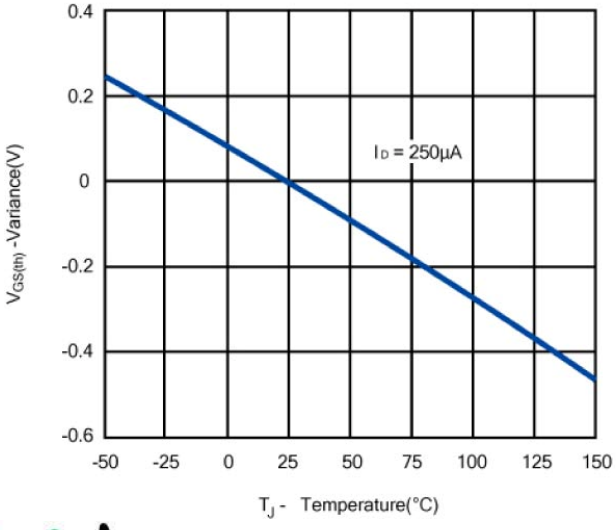
Capacitance



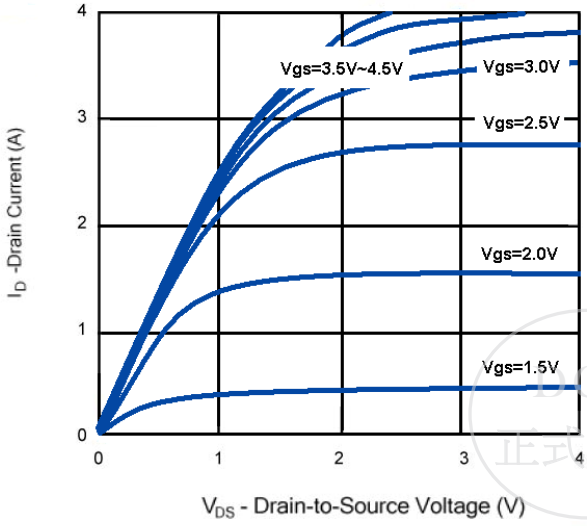
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



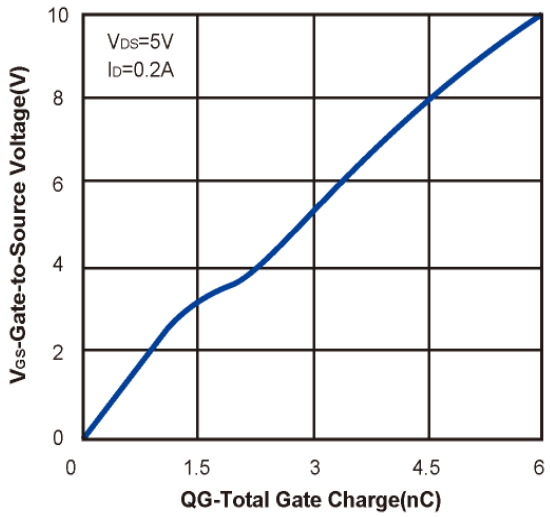
On-Region Characteristics



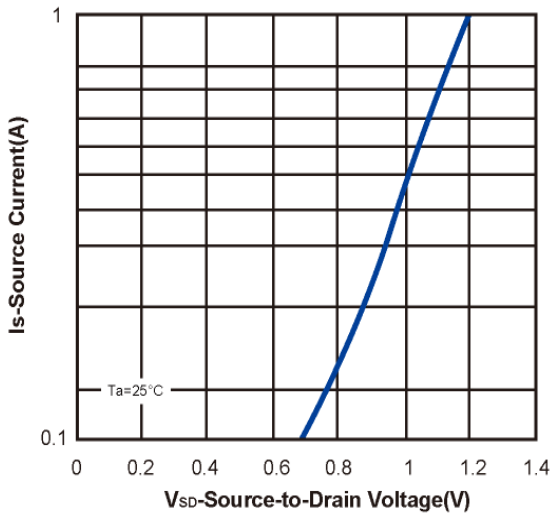
N-Channel 25V (D-S) MOSFET, ESD Protected

Typical Characteristics (T_J =25℃ Noted)

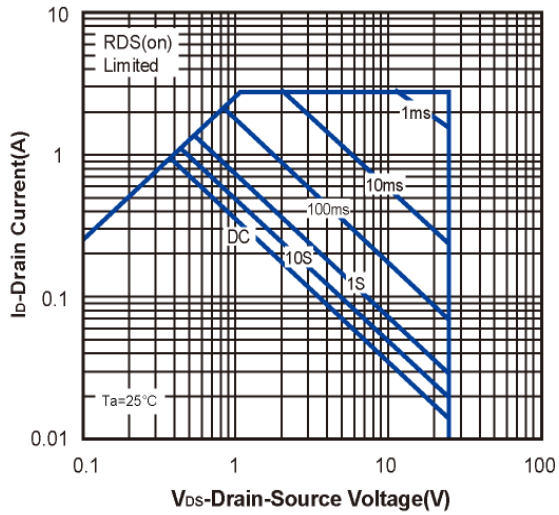
Gate Charge



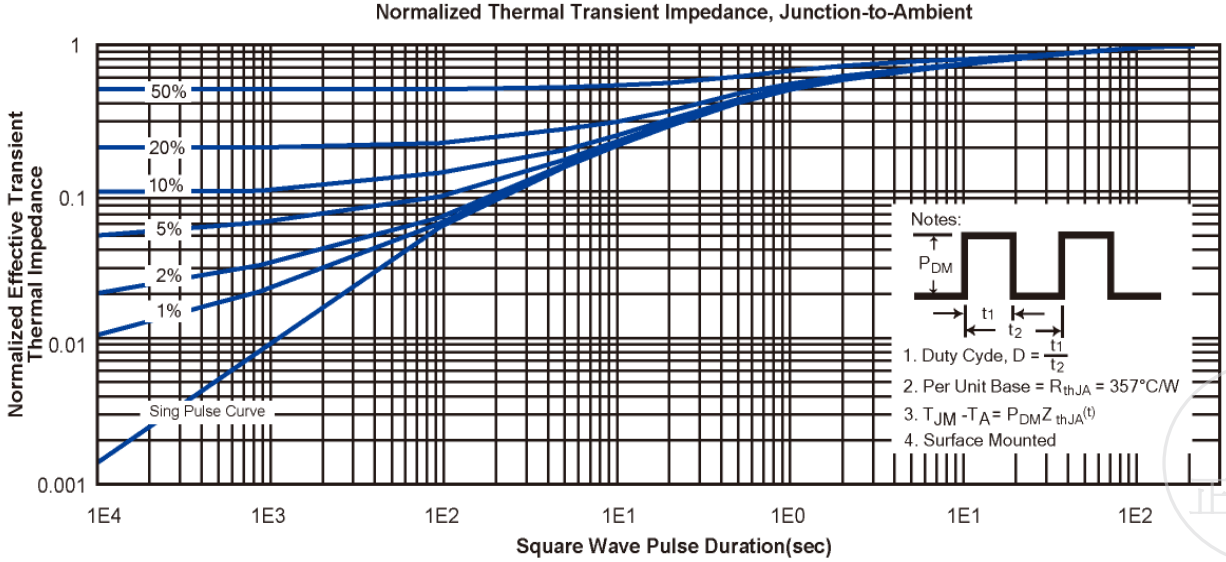
Body-diode characteristics



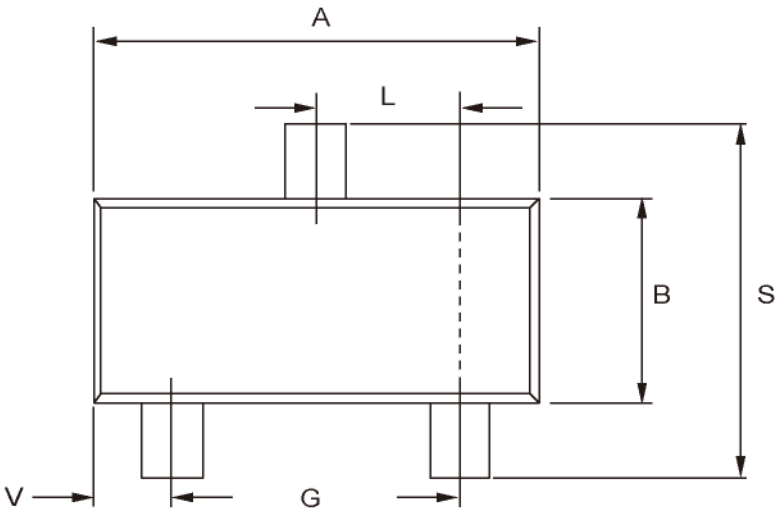
Maximum Forward Biased Safe Operating Area

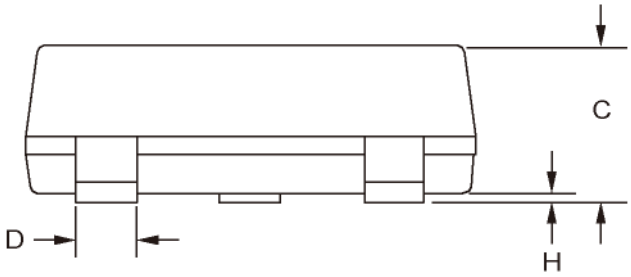


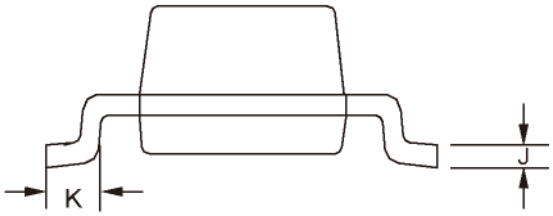
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60