

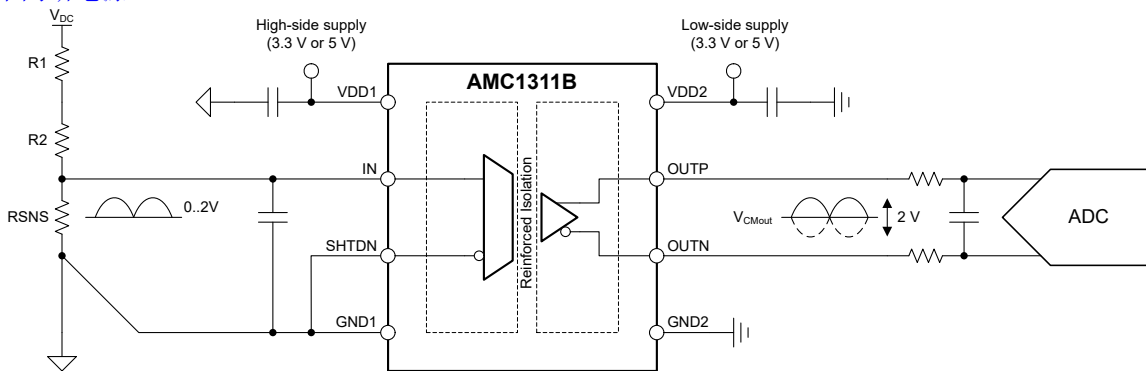
AMC1311x 高阻抗 2V 输入增强型隔离放大器

1 特性

- 针对隔离式电压测量优化了 2V 高阻抗输入电压范围
- 固定增益：1
- 低直流误差：
 - AMC1311：
 - 失调电压误差：±9.9mV (最大值)
 - 温漂±20 μV/°C (典型值)
 - 增益误差：±1% (最大值)
 - 增益漂移：±30ppm/°C (典型值)
 - AMC1311B：
 - 失调电压误差：±1.5mV (最大值)
 - 温漂±10 μV/°C (最大值)
 - 增益误差：±0.2% (最大值)
 - 增益漂移：±40ppm/°C (最大值)
- 非线性度：0.04% (最大值)
- 高侧 3.3V 工作电压 (AMC1311B)
- 高 CMTI：100kV/μs (最小值) (AMC1311B)
- 高侧电源缺失指示
- 安全相关认证：
 - 符合 DIN EN IEC 60747-17 (VDE 0884-17) 标准的 7000V_{PK} 增强型隔离
 - 符合 UL1577 标准且长达 1 分钟的 5000V_{RMS} 隔离
- 针对更大工业温度范围进行了全面优化：-40°C 至 +125°C

2 应用

- 可用于以下应用的隔离式电压感应：
 - 电机驱动器
 - 变频器
 - 不间断电源



简化版原理图

3 说明

AMC1311 是一款隔离式精密放大器，此放大器的输出与输入电路由抗电磁干扰性能极强的电容隔离层隔开。该隔离栅经认证可提供高达 5kV_{RMS} 的增强型电隔离，符合 DIN EN IEC 60747-17 (VDE 0884-17) 和 UL1577 标准，并且可支持高达 1500V_{RMS} 的工作电压。

该隔离层可将系统中以不同共模电压电平运行的各器件隔开，防止高电压冲击导致低压侧器件电气损坏或对操作员造成伤害。

AMC1311 的高阻抗输入针对与高阻抗电阻分压器或任何其他高阻抗电压信号源的连接进行了优化。出色的直流精度和低温漂支持在闭环系统中进行精确的隔离式电压检测和控制。集成的高侧电源电压缺失检测功能可简化系统级设计和诊断。

AMC1311 提供两种性能级别选项：AMC1311B 的额定工业工作温度范围为 -55°C 至 +125°C，AMC1311 为 -40°C 至 +125°C。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|----------|----------|-----------------|
| AMC1311 | SOIC (8) | 5.85mm × 7.50mm |
| AMC1311B | | |

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



Table of Contents

| | | | |
|--|----|--|----|
| 1 特性 | 1 | 8.1 Overview..... | 20 |
| 2 应用 | 1 | 8.2 Functional Block Diagram..... | 20 |
| 3 说明 | 1 | 8.3 Feature Description..... | 20 |
| 4 Revision History | 2 | 8.4 Device Functional Modes..... | 22 |
| 5 Device Comparison Table | 4 | 9 Application and Implementation | 23 |
| 6 Pin Configuration and Functions | 5 | 9.1 Application Information..... | 23 |
| 7 Specifications | 6 | 9.2 Typical Application..... | 23 |
| 7.1 Absolute Maximum Ratings..... | 6 | 9.3 What To Do and What Not To Do..... | 26 |
| 7.2 ESD Ratings..... | 6 | 10 Power Supply Recommendations | 27 |
| 7.3 Recommended Operating Conditions..... | 6 | 11 Layout | 28 |
| 7.4 Thermal Information..... | 7 | 11.1 Layout Guidelines..... | 28 |
| 7.5 Power Ratings..... | 7 | 11.2 Layout Example..... | 28 |
| 7.6 Insulation Specifications..... | 8 | 12 Device and Documentation Support | 29 |
| 7.7 Safety-Related Certifications..... | 9 | 12.1 Documentation Support..... | 29 |
| 7.8 Safety Limiting Values..... | 9 | 12.2 接收文档更新通知..... | 29 |
| 7.9 Electrical Characteristics..... | 10 | 12.3 支持资源..... | 29 |
| 7.10 Switching Characteristics..... | 12 | 12.4 Trademarks..... | 29 |
| 7.11 Timing Diagram..... | 12 | 12.5 Electrostatic Discharge Caution..... | 29 |
| 7.12 Insulation Characteristics Curves..... | 13 | 12.6 术语表..... | 29 |
| 7.13 Typical Characteristics..... | 14 | 13 Mechanical, Packaging, and Orderable Information | 29 |
| 8 Detailed Description | 20 | | |

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision B (May 2020) to Revision C (June 2022) | Page |
|--|------|
| • 将隔离标准从 DIN VDE V 0884-11 (VDE V 0884-11) 更改为 DIN EN IEC 60747-17 (VDE 0884-17)，并相应更新了绝缘规格和安全相关认证表..... | 1 |
| • 更改了特性部分..... | 1 |
| • Changed pin names: VIN to IN, VOUTP to OUTP, and VOUTN to OUTN..... | 5 |
| • Merged V _{OS} specs for 4.5V ≤ VDD1 ≤ 5.5 V and 3.0 V ≤ VDD1 ≤ 5.5 V ranges (AMC1311B only)..... | 10 |
| • Changed VDD1 DC PSRR from - 65 dB (typical) to - 80 dB (typical)..... | 10 |
| • Changed CMTI from 75 kV/μs (minimum), 140 kV/μs (typical) to 100 kV/μs (minimum), 150kV/μs (typical) (AMC1311B only)..... | 10 |
| • Changed VDD1 _{UV} (VDD1 falling) from 1.75 V / 2.53 V / 2.7 V to 2.4 V / 2.6 V / 2.8 V (minimum / typical / maximum)..... | 10 |
| • Changed <i>Rise, Fall, and Delay Time Definition</i> timing diagram..... | 12 |
| • Changed <i>Reinforced Isolation Capacitor Lifetime Projection</i> figure..... | 13 |
| • Changed functional block diagram..... | 20 |
| • Deleted <i>Fail-Safe Output</i> section, added <i>Analog Output</i> section..... | 22 |
| • Changed <i>Typical Application</i> section and subsections..... | 23 |
| • Changed <i>What To Do and What Not To Do</i> section..... | 26 |
| • Changed <i>Layout</i> section..... | 28 |

Changes from Revision A (June 2018) to Revision B (May 2020)

Page

| | |
|---|----|
| • 将特性部分的 AMC1311B 温漂从 $\pm 15 \mu V/^{\circ}C$ (最大值) 更改为 $10 \mu V/^{\circ}C$ (最大值) | 1 |
| • 将特性部分的 AMC1311B 增益误差从 $\pm 0.3\%$ (最大值) 更改为 $\pm 0.2\%$ (最大值), 并将 AMC1311B 增益漂 移从 $\pm 45 ppm/^{\circ}C$ (最大值) 更改为 $\pm 40 ppm/^{\circ}C$ (最大值) | 1 |
| • 将 IEC 60950-1 和 IEC60065 更改为 IEC 62368-1 | 1 |
| • Changed AMC1311B values for TCV_{OS} , E_G , and TCE_G in <i>Device Comparison Table</i> | 4 |
| • Changed AMC1311B values for TCV_{OS} , E_G , and TCE_G in <i>Device Comparison Table</i> | 6 |
| • Added ESD classification levels to <i>ESD Ratings</i> table..... | 6 |
| • Changed CLR and CPG values from 9 mm to 8.5 mm..... | 6 |
| • Changed <i>Insulation Specifications</i> table per ISO standard..... | 6 |
| • Changed <i>Safety-Related Certification</i> table per ISO standard..... | 6 |
| • Changed <i>Safety Limiting Values</i> description as per ISO standard..... | 6 |
| • Changed TCV_{OS} parameter minimum value from $-15 \mu V/^{\circ}C$ to $-10 \mu V/^{\circ}C$ and maximum value from $15 \mu V/^{\circ}C$ to $10 \mu V/^{\circ}C$ for the AMC1311B in the <i>Electrical Characteristics</i> table..... | 6 |
| • Changed E_G parameter minimum value from -0.3% to -0.2% and maximum value from 0.3% to 0.2% for the AMC1311B in the <i>Electrical Characteristics</i> table..... | 6 |
| • Changed TCE_G parameter minimum value from $-45 ppm/^{\circ}C$ to $-40 ppm/^{\circ}C$ and maximum value from $45 ppm/^{\circ}C$ to $40 ppm/^{\circ}C$ for the AMC1311B in the <i>Electrical Characteristics</i> table..... | 6 |
| • Changed <i>Step Response of the AMC1311</i> figure..... | 26 |

5 Device Comparison Table

| PARAMETER | | AMC1311B | AMC1311 |
|---|----------------------|-----------------------------------|------------------|
| High-side supply voltage, VDD1 | | 3.0 V to 5.5 V | 4.5 V to 5.5 V |
| Specified ambient temperature, T _A | | - 55°C to +125°C | - 40°C to +125°C |
| Input offset voltage, V _{OS} | 4.5 V ≤ VDD1 ≤ 5.5 V | ±1.5 mV | ±9.9 mV |
| | 3.0 V ≤ VDD1 ≤ 5.5 V | ±2.5 mV | Not applicable |
| Input offset drift, TCV _{OS} | | ±3 μV/°C (typ), ±10 μV/°C (max) | ±20 μV/°C (typ) |
| Gain error, E _G | | ±0.2% | ±1% |
| Gain error drift, TCE _G | | ±5 ppm/°C (typ), ±40 ppm/°C (max) | ±30 ppm/°C (typ) |
| Common-mode transient immunity, CMTI | | 100 kV/μs (min) | 15 kV/μs (min) |

6 Pin Configuration and Functions

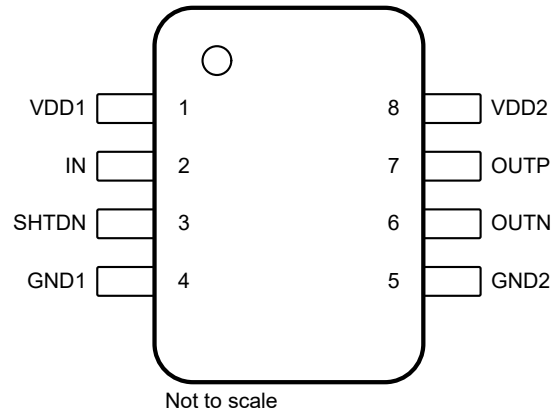


图 6-1. DWV Package, 8-Pin SOIC (Top View)

表 6-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----|-------|------------------|---|
| NO. | NAME | | |
| 1 | VDD1 | High-side power | High-side power supply ⁽¹⁾ |
| 2 | IN | Analog input | Analog input |
| 3 | SHTDN | Digital input | Shutdown input, active high, with internal pullup resistor (typical value: 100 k Ω) |
| 4 | GND1 | High-side ground | High-side analog ground |
| 5 | GND2 | Low-side ground | Low-side analog ground |
| 6 | OUTN | Analog output | Inverting analog output |
| 7 | OUTP | Analog output | Noninverting analog output |
| 8 | VDD2 | Low-side power | Low-side power supply ⁽¹⁾ |

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings

see⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------------|--|------------|------------|------|
| Power-supply voltage | High-side VDD1 to GND1 | - 0.3 | 6.5 | V |
| | Low-side VDD2 to GND2 | - 0.3 | 6.5 | |
| Input voltage | IN | GND1 - 6 | VDD1 + 0.5 | V |
| | SHTDN | GND1 - 0.5 | VDD1 + 0.5 | |
| Output voltage | OUTP, OUTN | GND2 - 0.5 | VDD2 + 0.5 | V |
| Input current | Continuous, any pin except power-supply pins | - 10 | 10 | mA |
| Temperature | Junction, T _J | | 150 | °C |
| | Storage, T _{stg} | - 65 | 150 | |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|--------------------------|--------------------------------------|-------------------------|-------|-----|------|------|
| POWER SUPPLY | | | | | | |
| | High-side power supply | VDD1 to GND1, AMC1311 | 4.5 | 5 | 5.5 | V |
| | | VDD1 to GND1, AMC1311B | 3 | 5 | 5.5 | |
| | Low-side power supply | VDD2 to GND2 | 3 | 3.3 | 5.5 | V |
| ANALOG INPUT | | | | | | |
| V _{Clipping} | Input voltage before clipping output | IN to GND1 | 2.516 | | | V |
| V _{FSR} | Specified linear full-scale voltage | IN to GND1 | - 0.1 | | 2 | V |
| ANALOG OUTPUT | | | | | | |
| C _{LOAD} | Capacitive load | On OUTP or OUTN to GND2 | | | 500 | pF |
| | | OUTP to OUTN | | | 250 | |
| R _{LOAD} | Resistive load | On OUTP or OUTN to GND2 | | 10 | 1 | kΩ |
| DIGITAL INPUT | | | | | | |
| | Input voltage | SHTDN to GND1 | 0 | | VDD1 | V |
| TEMPERATURE RANGE | | | | | | |
| T _A | Specified ambient temperature | AMC1311 | - 40 | | 125 | °C |
| | | AMC1311B | - 55 | | 125 | |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DWV (SOIC) | UNIT |
|-------------------------------|--|------------|------|
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 84.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 28.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 41.1 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 4.9 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 39.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|-----------|--|-----------------------------------|-------|------|
| P_D | Maximum power dissipation (both sides) | VDD1 = VDD2 = 5.5 V | 98 | mW |
| | | VDD1 = VDD2 = 3.6V, AMC1311B only | 56 | |
| P_{D1} | Maximum power dissipation (high-side) | VDD1 = 5.5 V | 53 | mW |
| | | VDD1 = 3.6 V, AMC1311B only | 30 | |
| P_{D2} | Maximum power dissipation (low-side) | VDD2 = 5.5 V | 45 | mW |
| | | VDD2 = 3.6 V, AMC1311B only | 26 | |

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|--|---|--|--------------------|------------------|
| GENERAL | | | | |
| CLR | External clearance ⁽¹⁾ | Shortest pin-to-pin distance through air | ≥ 8.5 | mm |
| CPG | External creepage ⁽¹⁾ | Shortest pin-to-pin distance across the package surface | ≥ 8.5 | mm |
| DTI | Distance through insulation | Minimum internal gap (internal clearance) of the double insulation | ≥ 0.021 | mm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | ≥ 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 1000 V _{RMS} | I-III | |
| DIN EN IEC 60747-17 (VDE 0884-17)⁽²⁾ | | | | |
| V _{IORM} | Maximum repetitive peak isolation voltage | At AC voltage | 2120 | V _{PK} |
| V _{IOWM} | Maximum-rated isolation working voltage | At AC voltage (sine wave) | 1500 | V _{RMS} |
| | | At DC voltage | 2120 | V _{DC} |
| V _{IOTM} | Maximum transient isolation voltage | V _{TEST} = V _{IOTM} , t = 60 s (qualification test) | 7000 | V _{PK} |
| | | V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test) | 8400 | |
| V _{IMP} | Maximum impulse voltage ⁽³⁾ | Tested in air, 1.2/50-μs waveform per IEC 62368-1 | 9800 | V _{PK} |
| V _{IOSM} | Maximum surge isolation voltage ⁽⁴⁾ | Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1 | 12800 | V _{PK} |
| q _{pd} | Apparent charge ⁽⁵⁾ | Method a, after input/output safety test subgroups 2 and 3, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s | ≤ 5 | pC |
| | | Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s | ≤ 5 | |
| | | Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s | ≤ 5 | |
| C _{IO} | Barrier capacitance, input to output ⁽⁶⁾ | V _{IO} = 0.5 V _{PP} at 1 MHz | ~1.5 | pF |
| R _{IO} | Insulation resistance, input to output ⁽⁶⁾ | V _{IO} = 500 V at T _A = 25°C | > 10 ¹² | Ω |
| | | V _{IO} = 500 V at 100°C ≤ T _A ≤ 125°C | > 10 ¹¹ | |
| | | V _{IO} = 500 V at T _S = 150°C | > 10 ⁹ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 55/125/21 | |
| UL1577 | | | | |
| V _{ISO} | Withstand isolation voltage | V _{TEST} = V _{ISO} = 5000 V _{RMS} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} = 6000 V _{RMS} , t = 1 s (100% production test) | 5000 | V _{RMS} |

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

| VDE | UL |
|---|---|
| DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9 | Recognized under 1577 component recognition |
| Reinforced insulation | Single protection |
| Certificate number: 40040142 | File number: E181974 |

7.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|--|-----|-----|------|------|
| I _S | Safety input, output, or supply current | R _{θJA} = 84.6°C/W, VDD _X = 5.5 V, T _J = 150°C, T _A = 25°C | | | 268 | mA |
| | | R _{θJA} = 84.6°C/W, VDD _X = 3.6 V, T _J = 150°C, T _A = 25°C, AMC1311B only | | | 410 | |
| P _S | Safety input, output, or total power | R _{θJA} = 84.6°C/W, T _J = 150°C, T _A = 25°C | | | 1477 | mW |
| T _S | Maximum safety temperature | | | | 150 | °C |

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.

T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum junction temperature.

P_S = I_S × VDD_{max}, where VDD_{max} is the maximum supply voltage for high-side and low-side.

7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1311 apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD1} = 4.5\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $V_{IN} = -0.1\text{ V}$ to 2 V , and $\text{SHTDN} = \text{GND1} = 0\text{ V}$; minimum and maximum specifications of the AMC1311B apply from $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $V_{IN} = -0.1\text{ V}$ to 2 V , and $\text{SHTDN} = \text{GND1} = 0\text{ V}$ (unless otherwise noted); typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|--|---------|--------------|-------|------------------------------|
| ANALOG INPUT | | | | | | |
| V_{OS} | Input offset voltage ^{(1) (2)} | $T_A = 25^\circ\text{C}$, $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, AMC1311 | - 9.9 | ± 0.4 | 9.9 | mV |
| | | $T_A = 25^\circ\text{C}$, AMC1311B ⁽³⁾ | - 1.5 | ± 0.4 | 1.5 | |
| TCV_{OS} | Input offset thermal drift ^{(1) (2) (5)} | AMC1311 | | ± 20 | | $\mu\text{V}/^\circ\text{C}$ |
| | | AMC1311B | - 10 | ± 3 | 10 | |
| R_{IN} | Input resistance | $T_A = 25^\circ\text{C}$ | | 1 | | $\text{G}\Omega$ |
| I_{IB} | Input bias current | $I_N = \text{GND1}$, $T_A = 25^\circ\text{C}$ | - 15 | 3.5 | 15 | nA |
| C_{IN} | Input capacitance | $f_{IN} = 275\text{ kHz}$ | | 7 | | pF |
| ANALOG OUTPUT | | | | | | |
| | Nominal gain | | | 1 | | V/V |
| E_G | Gain error ⁽¹⁾ | $T_A = 25^\circ\text{C}$, AMC1311 | - 1% | 0.4% | 1% | |
| | | $T_A = 25^\circ\text{C}$, AMC1311B | - 0.2% | $\pm 0.05\%$ | 0.2% | |
| TCE_G | Gain error drift ^{(1) (6)} | AMC1311 | | ± 30 | | ppm/ $^\circ\text{C}$ |
| | | AMC1311B | - 40 | ± 5 | 40 | |
| | Nonlinearity ⁽¹⁾ | | - 0.04% | $\pm 0.01\%$ | 0.04% | |
| THD | Total harmonic distortion ⁽⁴⁾ | $V_{IN} = 2 V_{PP}$, $V_{IN} > 0\text{ V}$, $f_{IN} = 10\text{ kHz}$, $\text{BW} = 10\text{ kHz}$ | | - 87 | | dB |
| SNR | Signal-to-noise ratio | $V_{IN} = 2 V_{PP}$, $f_{IN} = 1\text{ kHz}$, $\text{BW} = 10\text{ kHz}$ | 79 | 82.6 | | dB |
| | | $V_{IN} = 2 V_{PP}$, $f_{IN} = 10\text{ kHz}$, $\text{BW} = 100\text{ kHz}$ | | 70.9 | | |
| | Output noise | $V_{IN} = \text{GND1}$, $\text{BW} = 100\text{ kHz}$ | | 220 | | μV_{rms} |
| PSRR | Power-supply rejection ratio ⁽²⁾ | vs V_{DD1} , at DC | | - 80 | | dB |
| | | vs V_{DD2} , at DC | | - 85 | | |
| | | vs V_{DD1} , 10 kHz / 100-mV ripple | | - 65 | | |
| | | vs V_{DD2} , 10 kHz / 100-mV ripple | | - 70 | | |
| V_{CMout} | Output common-mode voltage | | 1.39 | 1.44 | 1.49 | V |
| $V_{CLIPout}$ | Clipping differential output voltage | $V_{OUT} = (V_{OUTP} - V_{OUTN})$; $V_{IN} > V_{Clipping}$ | | 2.49 | | V |
| $V_{FAILSAFE}$ | Failsafe differential output voltage | $\text{SHTDN} = \text{high}$, or V_{DD1} undervoltage, or V_{DD1} missing | | - 2.6 | - 2.5 | V |
| BW | Output bandwidth | AMC1311 | 100 | 220 | | kHz |
| | | AMC1311B | 220 | 275 | | |
| R_{OUT} | Output resistance | On OUTP or OUTN | | <0.2 | | Ω |
| | Output short-circuit current | On OUTP or OUTN , sourcing or sinking, $I_N = \text{GND1}$, outputs shorted to either GND or V_{DD2} | | 14 | | mA |
| CMTI | Common-mode transient immunity | AMC1311 | 15 | 30 | | kV/ μs |
| | | AMC1311B | 100 | 150 | | |

7.9 Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1311 apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD1} = 4.5\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $V_{IN} = -0.1\text{ V}$ to 2 V , and $\text{SHTDN} = \text{GND1} = 0\text{ V}$; minimum and maximum specifications of the AMC1311B apply from $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $V_{IN} = -0.1\text{ V}$ to 2 V , and $\text{SHTDN} = \text{GND1} = 0\text{ V}$ (unless otherwise noted); typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---------------------------------------|--|--------------------------|------|--------------------------|---------------|
| DIGITAL INPUT | | | | | | |
| I_{IN} | Input current | $\text{SHTDN pin}, \text{GND1} \leq \text{SHTDN} \leq \text{VDD1}$ | -70 | | 1 | μA |
| C_{IN} | Input capacitance | SHTDN pin | | 5 | | pF |
| V_{IH} | High-level input voltage | | $0.7 \times \text{VDD1}$ | | | V |
| V_{IL} | Low-level input voltage | | | | $0.3 \times \text{VDD1}$ | V |
| POWER SUPPLY | | | | | | |
| V_{DD1UV} | VDD1 undervoltage detection threshold | VDD1 rising | 2.5 | 2.7 | 2.9 | V |
| | | VDD1 falling | 2.4 | 2.6 | 2.8 | |
| V_{DD2UV} | VDD2 undervoltage detection threshold | VDD2 rising | 2.2 | 2.45 | 2.65 | V |
| | | VDD2 falling | 1.85 | 2.0 | 2.2 | |
| I_{DD1} | High-side supply current | $3.0\text{ V} < \text{VDD1} < 3.6\text{ V}, \text{SHTDN} = \text{low}, \text{AMC1311B only}$ | | 6.0 | 8.4 | mA |
| | | $4.5\text{ V} < \text{VDD1} < 5.5\text{ V}, \text{SHTDN} = \text{low}$ | | 7.1 | 9.7 | |
| | | $\text{SHTDN} = \text{VDD1}$ | | 1.3 | | μA |
| I_{DD2} | Low-side supply current | $3.0\text{ V} < \text{VDD2} < 3.6\text{ V}$ | | 5.3 | 7.2 | mA |
| | | $4.5\text{ V} < \text{VDD2} < 5.5\text{ V}$ | | 5.9 | 8.1 | |

- (1) The typical value includes one standard deviation (σ) at nominal operating conditions.
- (2) This parameter is input referred.
- (3) The typical value is at $V_{DD1} = 3.3\text{ V}$.
- (4) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
- (5) Offset error temperature drift is calculated using the box method, as described by the following equation:

$$TCV_{OS} = (\text{Value}_{MAX} - \text{Value}_{MIN}) / \text{TempRange}$$
- (6) Gain error temperature drift is calculated using the box method, as described by the following equation:

$$TCE_G (\text{ppm}) = (\text{Value}_{MAX} - \text{Value}_{MIN}) / (\text{Value}_{(T=25^\circ\text{C})} \times \text{TempRange}) \times 10^6$$

7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|-------------------------------------|--|-----|-----|-----|---------------|
| t_r | Output signal rise time | | | 1.3 | | μs |
| t_f | Output signal fall time | | | 1.3 | | μs |
| | IN to OUTx signal delay (50% - 10%) | Unfiltered output, AMC1311 | | 1.5 | 2.5 | μs |
| | | Unfiltered output, AMC1311B | | 1.0 | 1.5 | |
| | IN to OUTx signal delay (50% - 50%) | Unfiltered output, AMC1311 | | 2.1 | 3.1 | μs |
| | | Unfiltered output, AMC1311B | | 1.6 | 2.1 | |
| | IN to OUTx signal delay (50% - 90%) | Unfiltered output, AMC1311 | | 3.0 | 4.0 | μs |
| | | Unfiltered output, AMC1311B | | 2.5 | 3.0 | |
| t_{AS} | Analog settling time | VDD1 step to 3.0 V with VDD2 \geq 3.0 V, to V _{OUTP} , V _{OUTN} valid, 0.1% settling | | 50 | 100 | μs |
| t_{EN} | Device enable time | SHTDN high to low | | 50 | 100 | μs |
| t_{SHTDN} | Device shutdown time | SHTDN low to high | | 3 | 10 | μs |

7.11 Timing Diagram

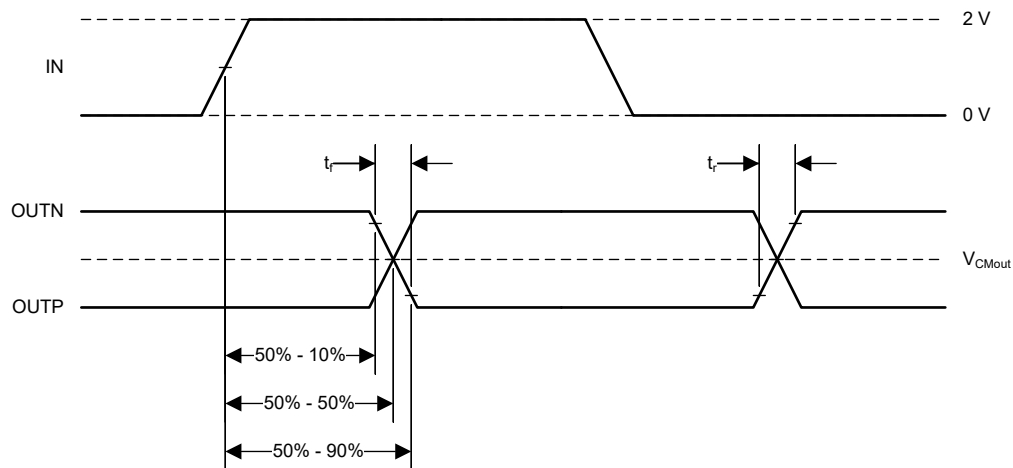


图 7-1. Rise, Fall, and Delay Time Definition

7.12 Insulation Characteristics Curves

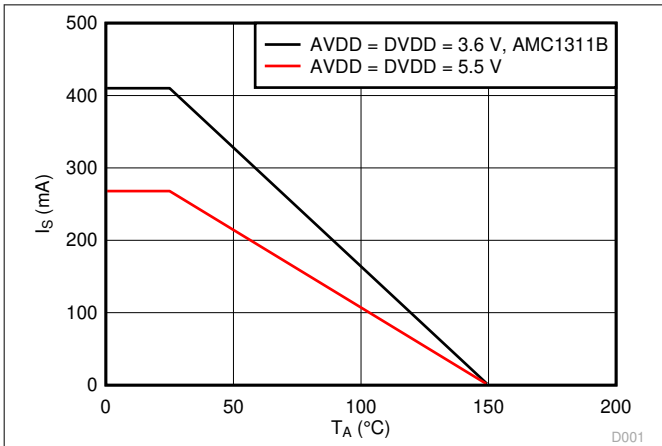


图 7-2. Thermal Derating Curve for Safety-Limiting Current per VDE

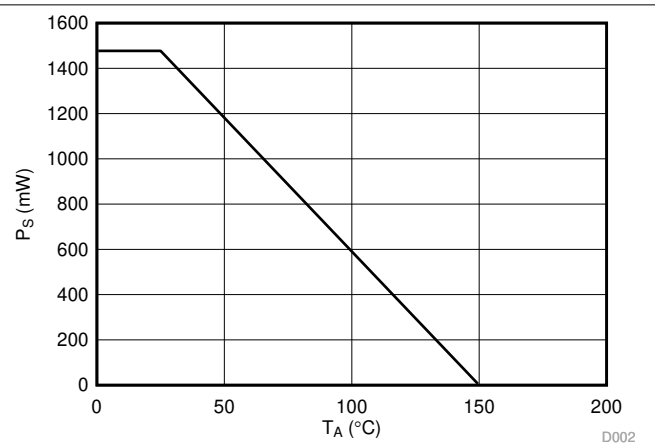


图 7-3. Thermal Derating Curve for Safety-Limiting Power per VDE

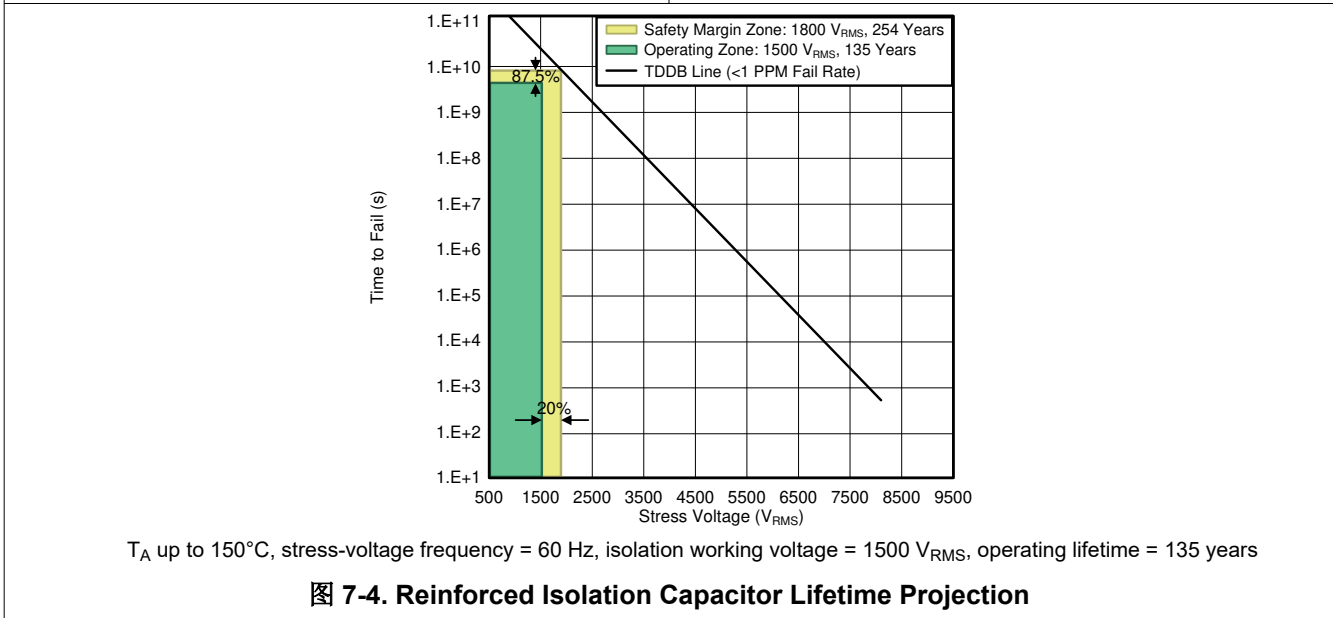


图 7-4. Reinforced Isolation Capacitor Lifetime Projection

7.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, $f_{IN} = 10$ kHz, and BW = 100 kHz (unless otherwise noted)

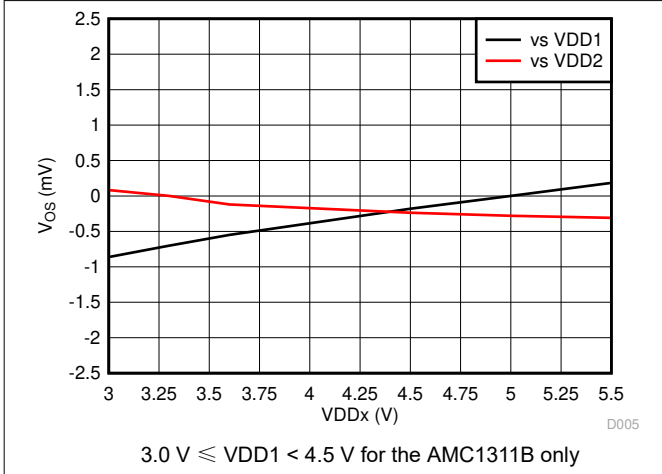


图 7-5. Input Offset Voltage vs Supply Voltage

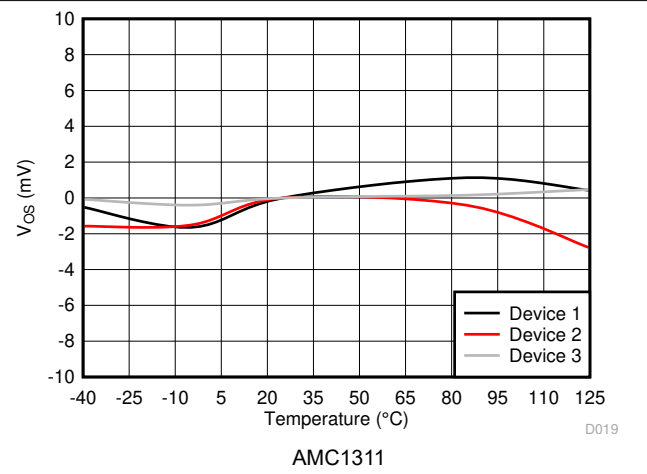


图 7-6. Input Offset Voltage vs Temperature

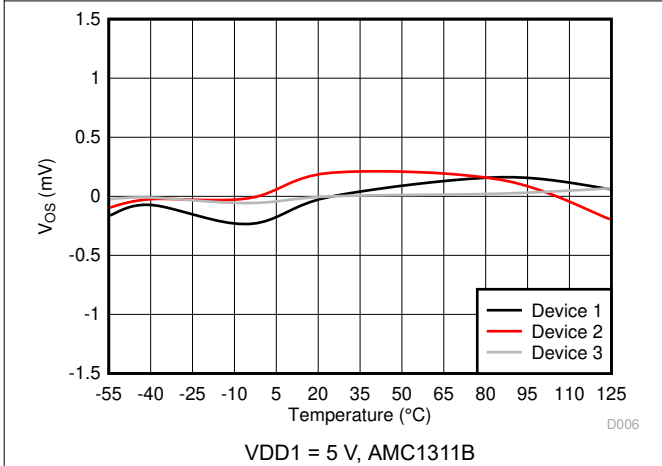


图 7-7. Input Offset Voltage vs Temperature

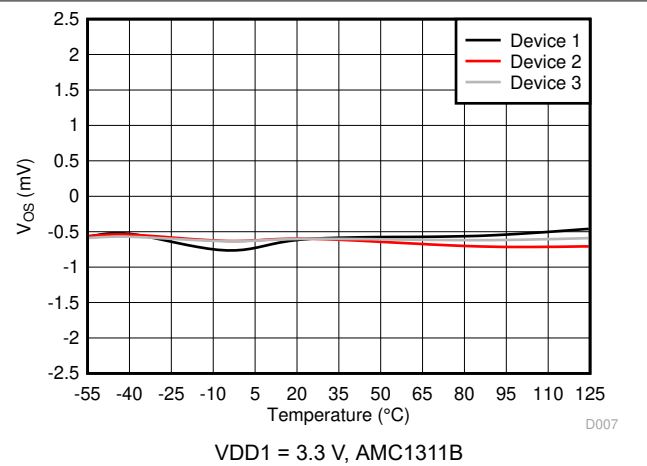


图 7-8. Input Offset Voltage vs Temperature

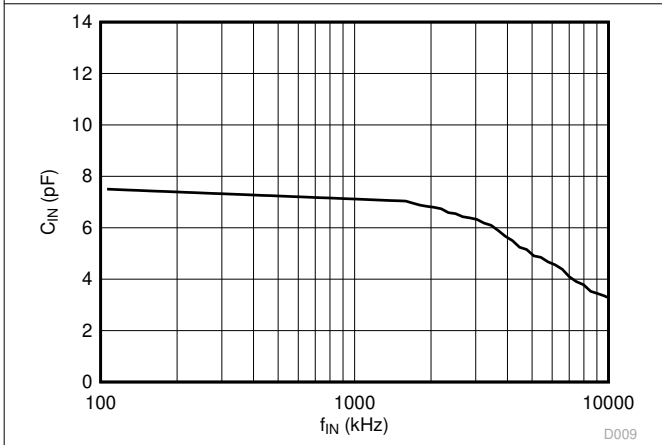


图 7-9. Input Capacitance vs Input Signal Frequency

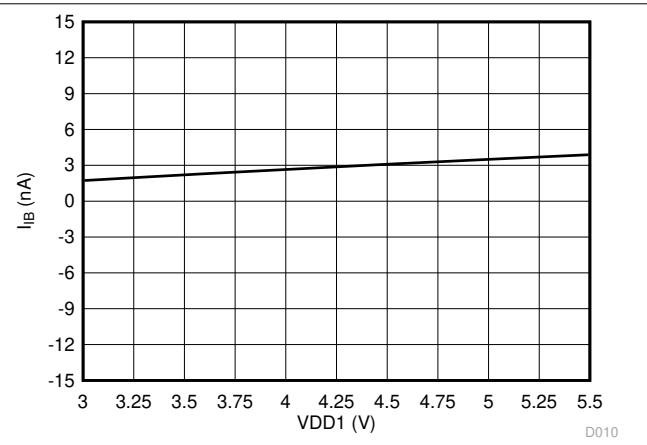
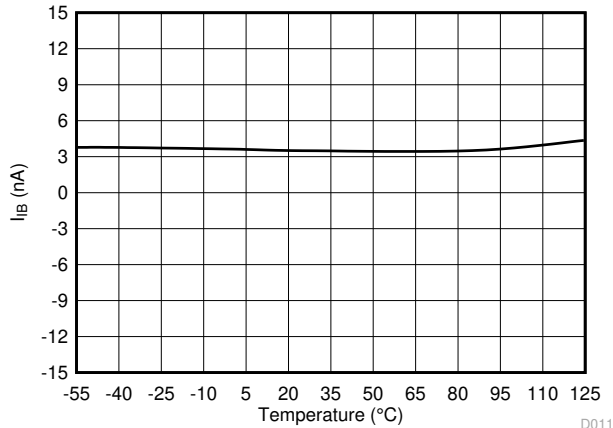


图 7-10. Input Bias Current vs High-Side Supply Voltage

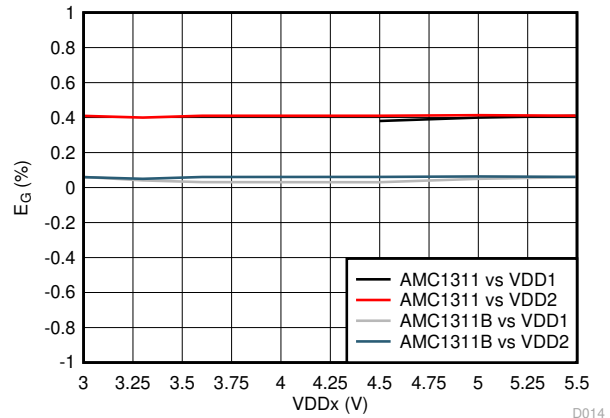
7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



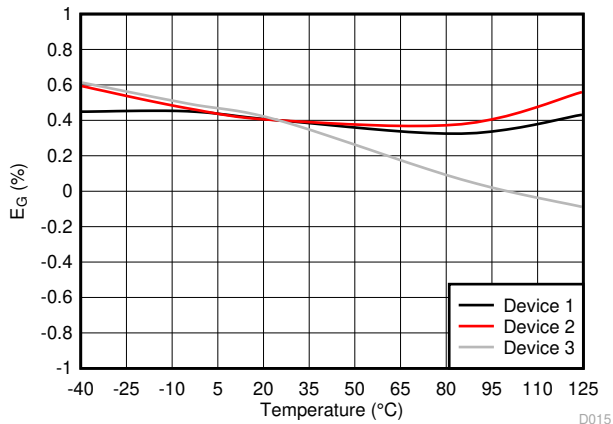
- 55°C ≤ T_A < - 40°C for the AMC1311B only

图 7-11. Input Bias Current vs Temperature



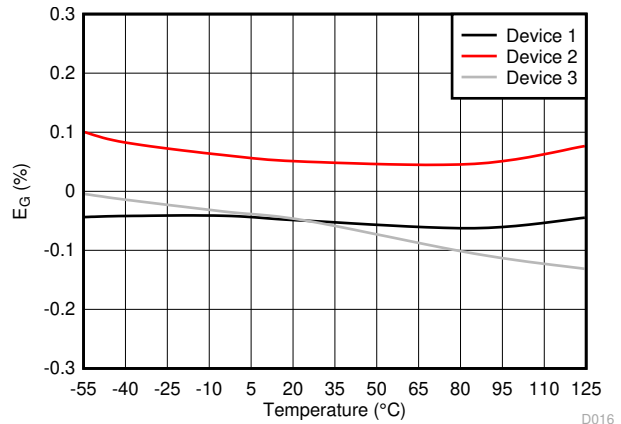
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

图 7-12. Gain Error vs Supply Voltage



AMC1311

图 7-13. Gain Error vs Temperature



AMC1311B

图 7-14. Gain Error vs Temperature

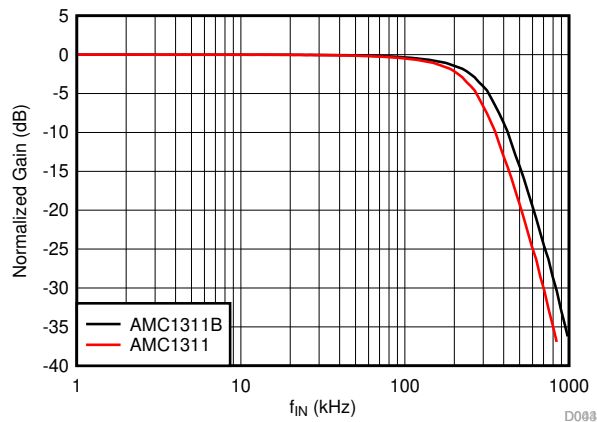


图 7-15. Normalized Gain vs Input Frequency

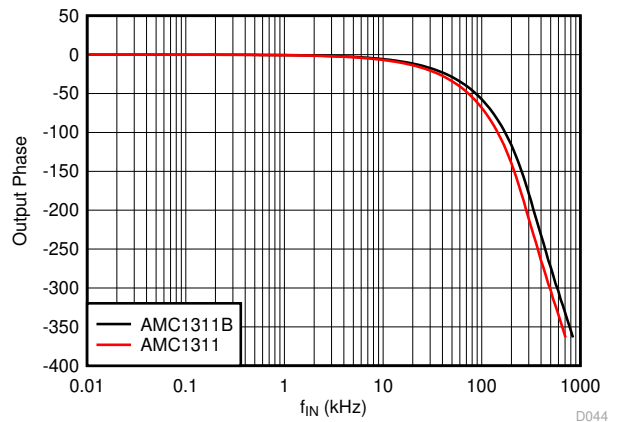


图 7-16. Output Phase vs Input Frequency

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

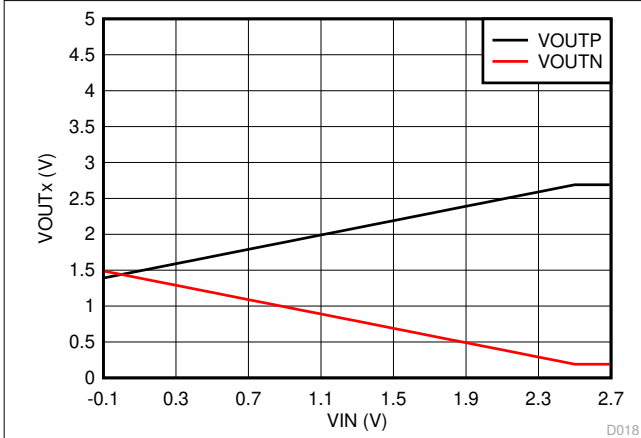


图 7-17. Output Voltage vs Input Voltage

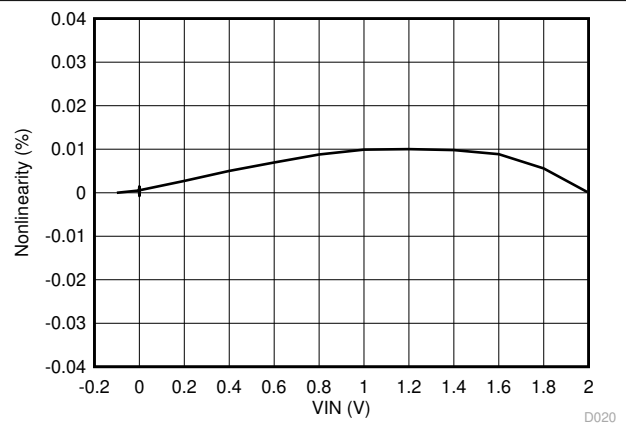
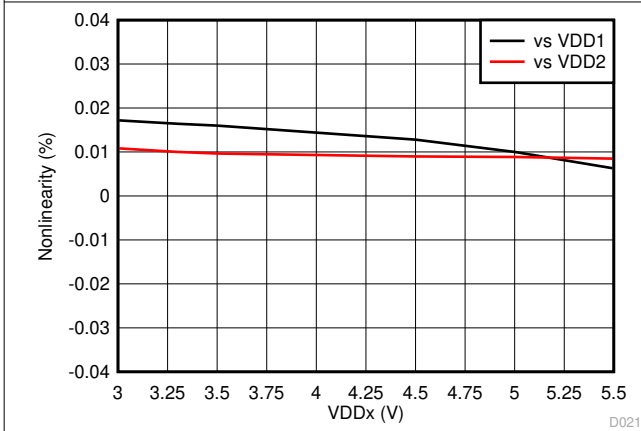
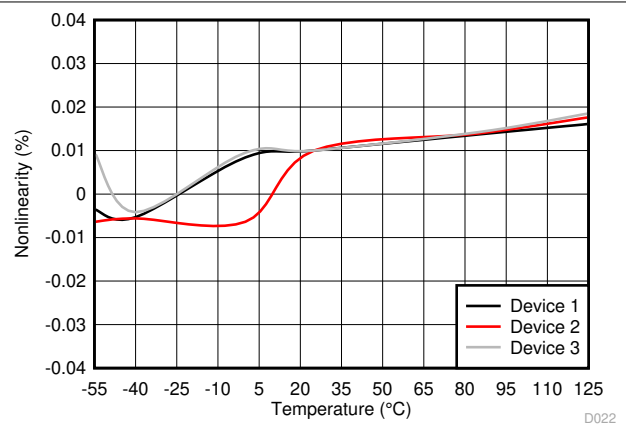


图 7-18. Nonlinearity vs Input Voltage



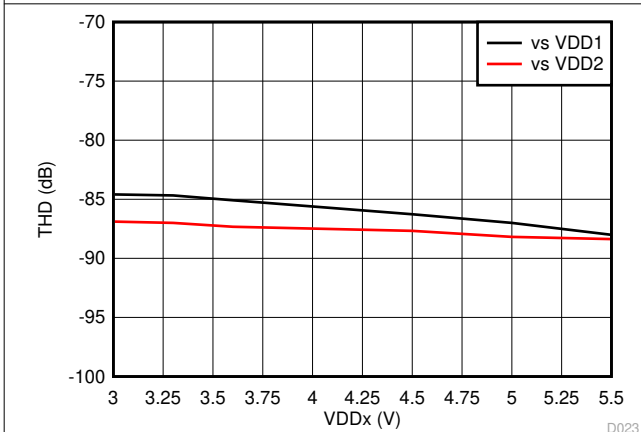
$3.0\text{ V} \leq \text{VDD1} < 4.5\text{ V}$ for the AMC1311B only

图 7-19. Nonlinearity vs Supply Voltage



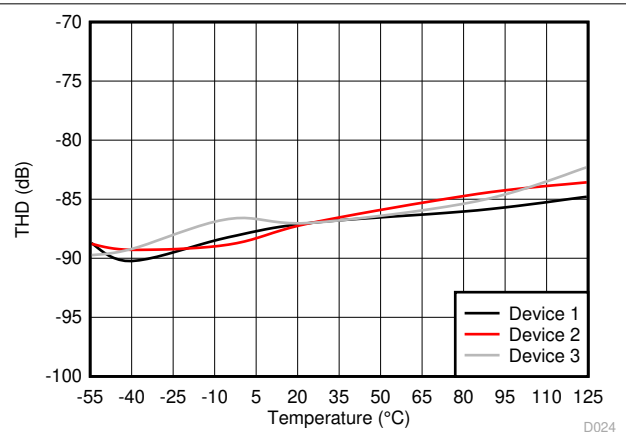
$-55^{\circ}\text{C} \leq T_A < -40^{\circ}\text{C}$ for the AMC1311B only

图 7-20. Nonlinearity vs Temperature



$3.0\text{ V} \leq \text{VDD1} < 4.5\text{ V}$ for the AMC1311B only

图 7-21. Total Harmonic Distortion vs Supply Voltage



$-55^{\circ}\text{C} \leq T_A < -40^{\circ}\text{C}$ for the AMC1311B only

图 7-22. Total Harmonic Distortion vs Temperature

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

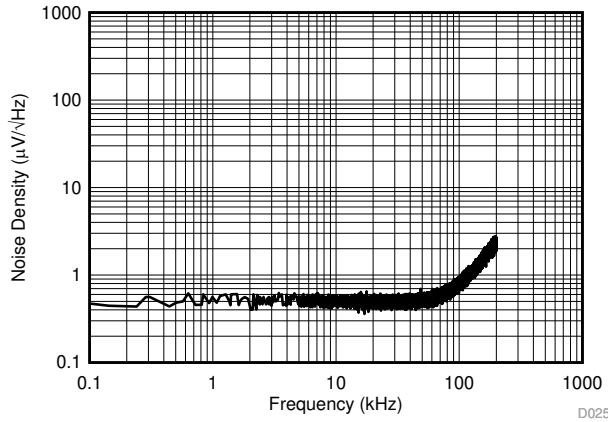


图 7-23. Input-Referred Noise Density vs Frequency

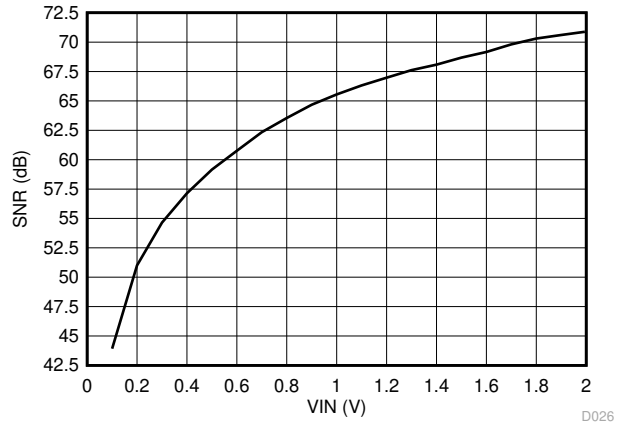
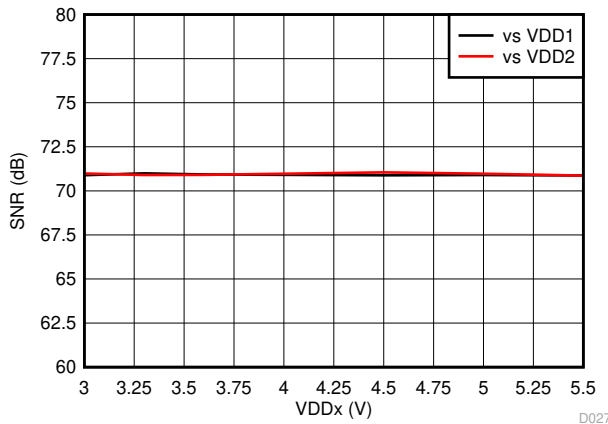
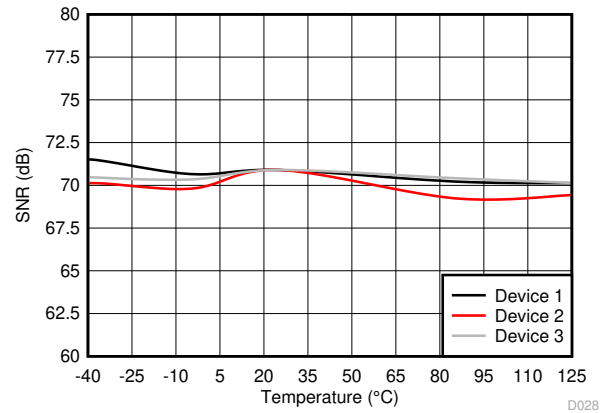


图 7-24. Signal-to-Noise Ratio vs Input Voltage



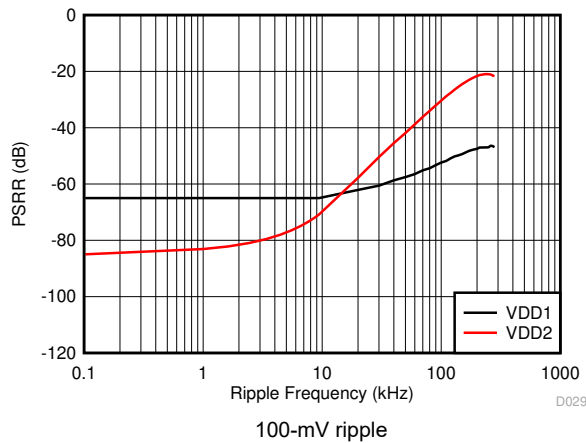
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

图 7-25. Signal-to-Noise Ratio vs Supply Voltage



-55°C ≤ T_A < -40°C for the AMC1311B only

图 7-26. Signal-to-Noise Ratio vs Temperature



100-mV ripple

图 7-27. Power-Supply Rejection Ratio vs Ripple Frequency

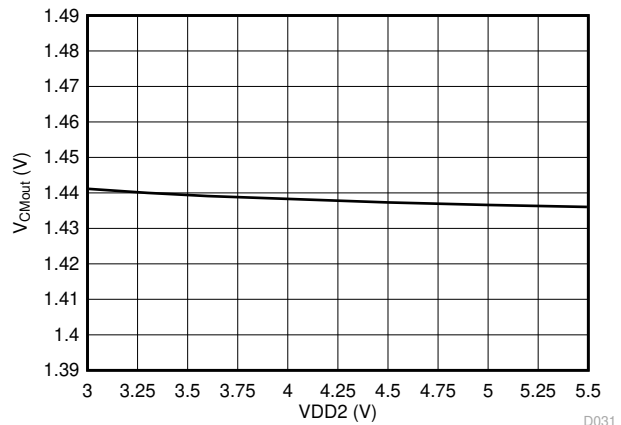
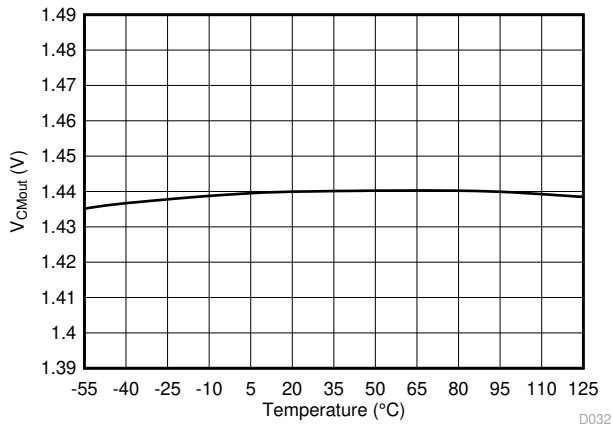


图 7-28. Output Common-Mode Voltage vs Low-Side Supply Voltage

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, $f_{IN} = 10$ kHz, and BW = 100 kHz (unless otherwise noted)



- 55°C ≤ T_A < - 40°C for the AMC1311B only

图 7-29. Output Common-Mode Voltage vs Temperature

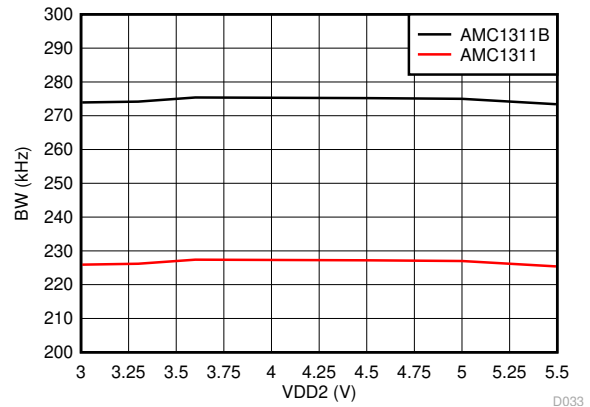


图 7-30. Output Bandwidth vs Low-Side Supply Voltage

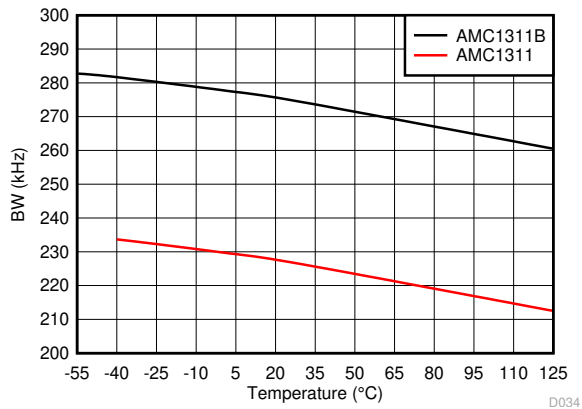
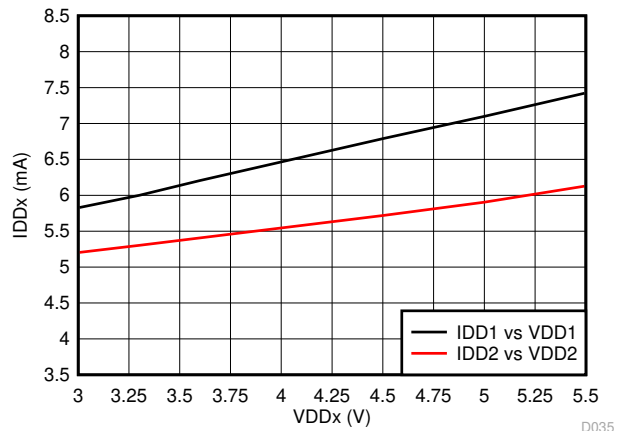
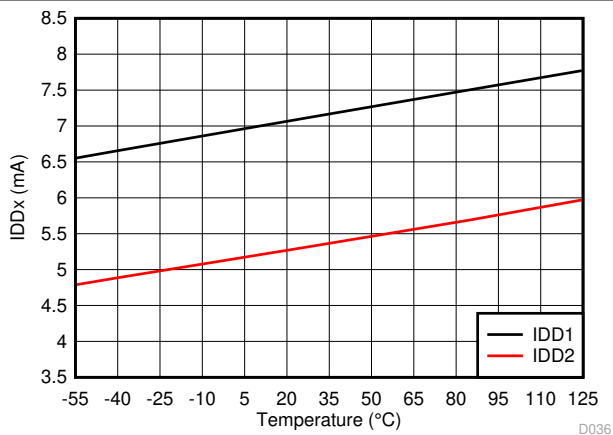


图 7-31. Output Bandwidth vs Temperature



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

图 7-32. Supply Current vs Supply Voltage



- 55°C ≤ T_A < - 40°C for the AMC1311B only

图 7-33. Supply Current vs Temperature

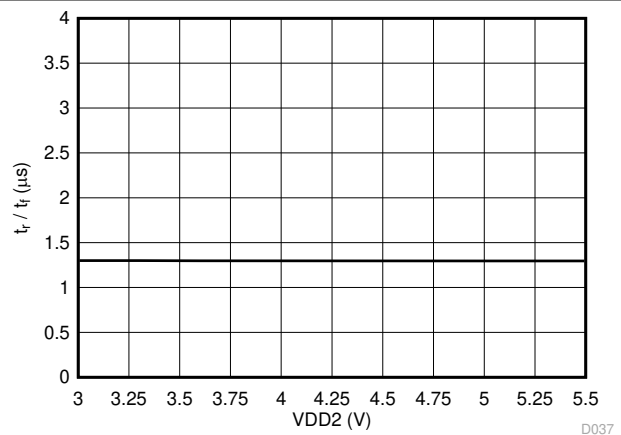


图 7-34. Output Rise and Fall Time vs Low-Side Supply Voltage

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, $f_{IN} = 10$ kHz, and BW = 100 kHz (unless otherwise noted)

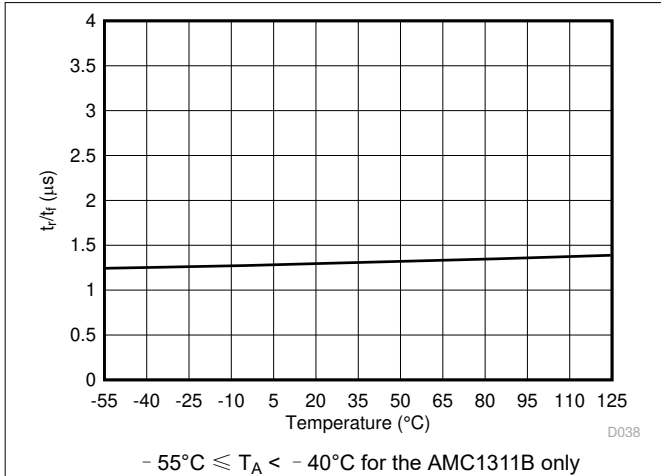


图 7-35. Output Rise and Fall Time vs Temperature

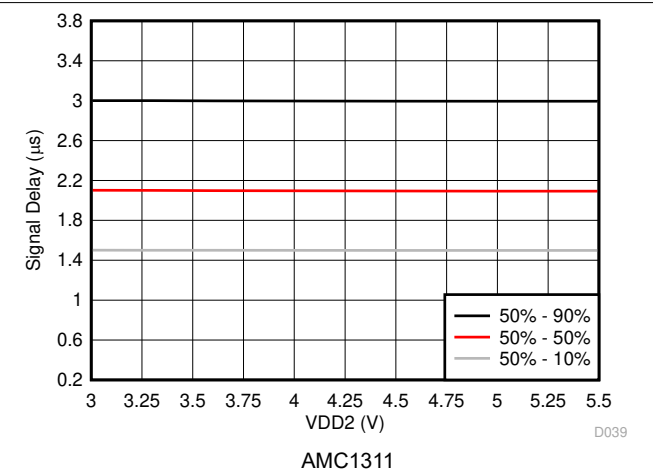


图 7-36. IN to OUTP, OUTN Signal Delay vs Low-Side Supply Voltage

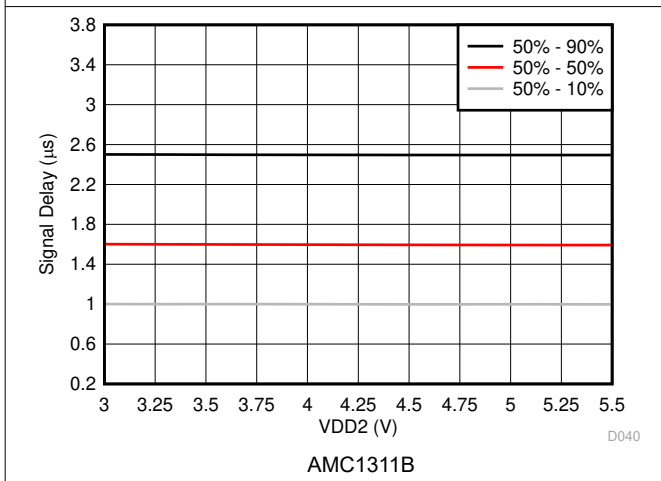


图 7-37. IN to OUTP, OUTN Signal Delay vs Low-Side Supply Voltage

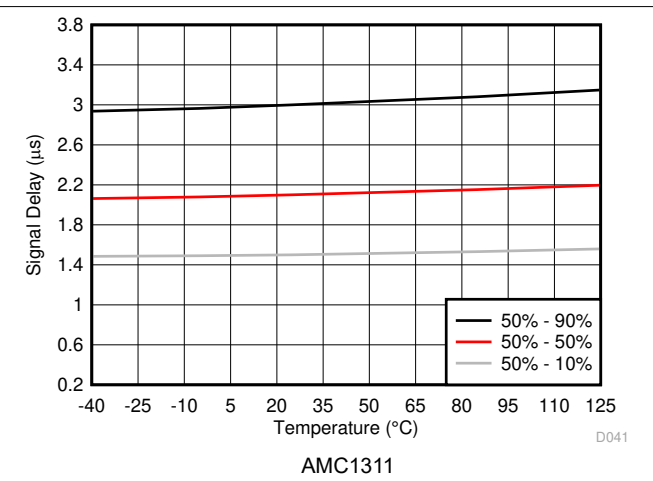


图 7-38. IN to OUTP, OUTN Signal Delay vs Temperature

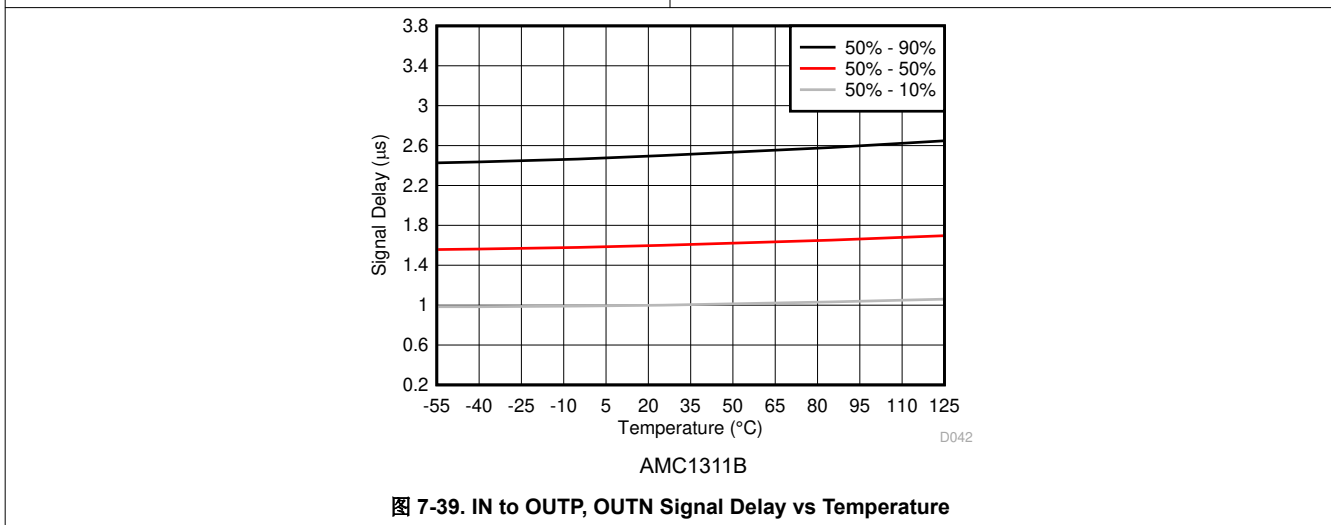


图 7-39. IN to OUTP, OUTN Signal Delay vs Temperature

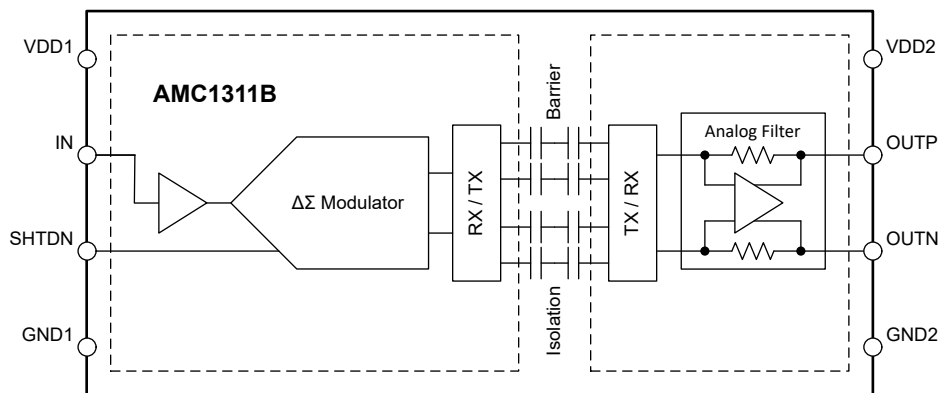
8 Detailed Description

8.1 Overview

The AMC1311 is a precision, single-ended input, isolated amplifier with a high input impedance and wide input voltage range. The input stage of the device drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier and separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUP and OUTN pins proportional to the input signal.

The SiO₂-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application report](#). The digital modulation used in the AMC1311 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and high common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The single-ended, high-impedance input stage of the AMC1311 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

There are two restrictions on the analog input signal IN. First, if the input voltage V_{IN} exceeds the range specified in the [Absolute Maximum Ratings](#) table, the input current must be limited to the absolute maximum value because the electrostatic discharge (ESD) protection turns on. Secondly, the linearity and parametric performance of the device is ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) as specified in the [Recommended Operating Conditions](#) table.

8.3.2 Isolation Channel Signal Transmission

The AMC1311 uses an on-off keying (OOK) modulation scheme, as shown in [图 8-1](#), to transmit the modulator output bitstream across the SiO₂-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1311 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1311 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

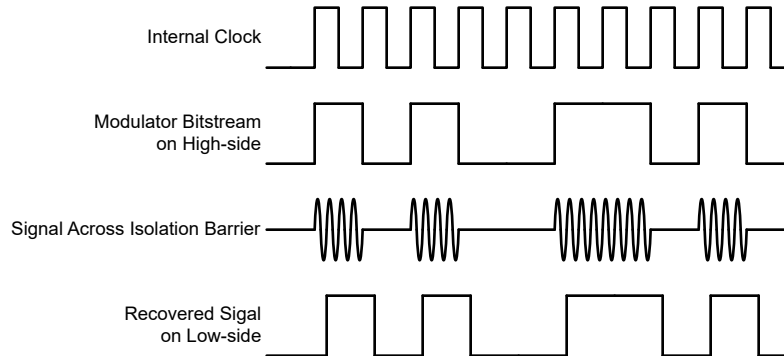


图 8-1. OOK-Based Modulation Scheme

8.3.3 Analog Output

The AMC1311 provides a differential analog output on the OOUTP and OOUTN pins. For input voltages of V_{IN} in the range from -0.1 V to $+2\text{ V}$, the device provides a linear response with a nominal gain of 1. For example, for an input voltage of 2 V , the differential output voltage ($V_{OOUTP} - V_{OOUTN}$) is 2 V . At zero input (IN shorted to GND1), both pins output the same common-mode output voltage V_{CMout} , as specified in the [Electrical Characteristics](#) table. For input voltages greater than 2 V but less than approximately 2.5 V , the differential output voltage continues to increase but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in [Figure 8-2](#), if the input voltage exceeds the $V_{Clipping}$ value.

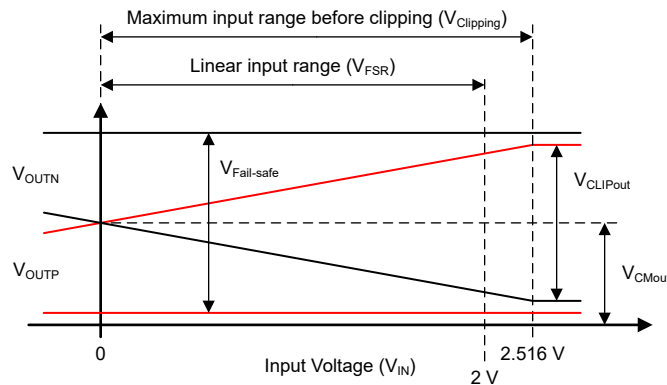


图 8-2. Output Behavior of the AMC1311

The AMC1311 output offers a fail-safe feature that simplifies diagnostics on a system level. [Figure 8-2](#) shows the fail-safe mode, in which the AMC1311 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in three cases:

- When the high-side supply VDD1 of the AMC1311 device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold $VDD1_{UV}$
- When the SHTDN pin is pulled high

Use the maximum $V_{Fail-safe}$ voltage specified in the [Electrical Characteristics](#) table as a reference value for fail-safe detection on a system level.

8.4 Device Functional Modes

The AMC1311 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the [Recommended Operating Conditions](#) table.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The high input impedance, low input bias current, low AC and DC errors, and low temperature drift make the AMC1311 a high-performance solution for industrial applications where voltage sensing in the presence of high common-mode voltage levels is required.

9.2 Typical Application

图 9-1 shows the AMC1311 in a typical application. The DC bus voltage is divided down to an approximate 2-V level across the bottom resistor (RSNS) of a high-impedance resistive divider that is sensed by the AMC1311. The AMC1311 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents this signal as a differential voltage signal on the output pins.

The high-impedance input and the high common-mode transient immunity (CMTI) of the AMC1311 ensure reliable and accurate operation even in high-noise environments.

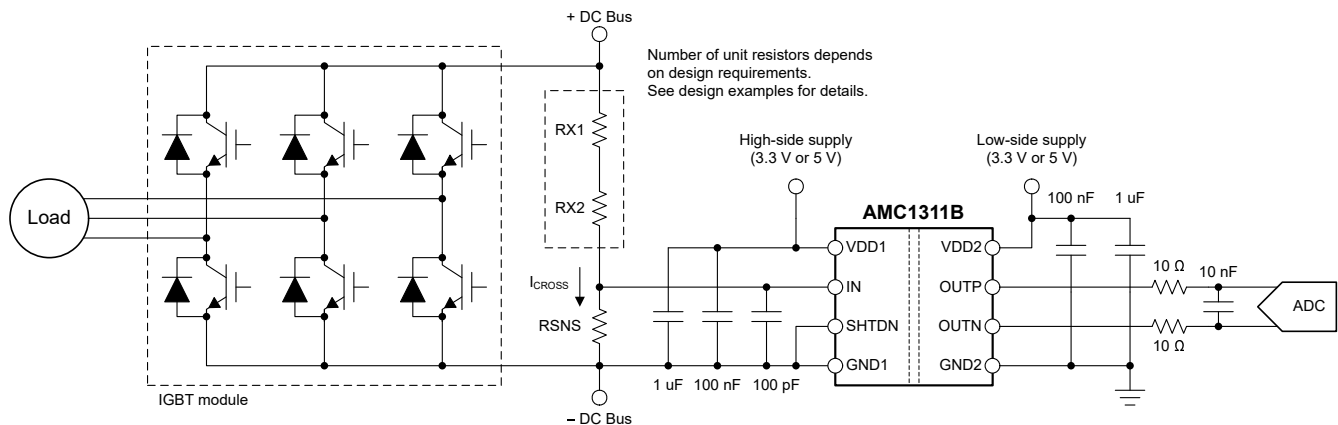


图 9-1. Using the AMC1311 for DC Link Voltage Sensing in Frequency Inverters

9.2.1 Design Requirements

表 9-1 lists the parameters for this typical application.

表 9-1. Design Requirements

| PARAMETER | VALUE |
|---|----------------------------|
| System input voltage | Single phase, 230 V, 50 Hz |
| Maximum DC link voltage | 400 V |
| High-side supply voltage | 3.3 V or 5 V |
| Low-side supply voltage | 3.3 V or 5 V |
| Maximum resistor operating voltage | 75 V |
| Voltage drop across the sense resistor (RSNS) for a linear response | 2 V (maximum) |
| Current through the resistive divider, I _{CROSS} | 100 μA (maximum) |

9.2.2 Detailed Design Procedure

The 100-μA, cross-current requirement at the maximum DC link voltage (400 V) determines that the total impedance of the resistive divider is 4 MΩ. The impedance of the resistive divider is dominated by the top portion (shown exemplary as RX1 and RX2 in 图 9-1) and the voltage drop across RSNS can be neglected for a moment. The maximum allowed voltage drop per unit resistor is specified as 75 V; therefore, the minimum number of unit resistors in the top portion of the resistive divider is 400 V / 75 V = 6. The calculated unit value is 4 MΩ / 6 = 666 kΩ and the next closest value from the E96 series is 665 kΩ.

RSNS is sized such that the voltage drop across the resistor at the maximum DC link voltage (400 V) equals the linear full-scale range input voltage (V_{FSR}) of the AMC1311, which is 2 V. This voltage is calculated as $RSNS = V_{FSR} / (V_{DC-link, max} - V_{FSR}) \times R_{TOP}$, where R_{TOP} is the total value of the top resistor string (6 × 665 kΩ = 3990 kΩ). RSNS is calculated as 20.05 kΩ and matches a value from the E96 series.

表 9-2. Resistor Value Example

| PARAMETER | VALUE |
|--|----------|
| Unit resistor R _x | 665 kΩ |
| Number of unit resistors | 6 |
| Sense resistor RSNS | 20.05 kΩ |
| Resulting current through resistive divider I _{CROSS} | 99.7 μA |
| Resulting voltage drop across sense resistor | 2.000 V |
| Power dissipated in unit resistor RX | 6.6 mW |
| Total power dissipated in resistive divider | 39.9 mW |

9.2.2.1 Input Filter Design

Placing an RC filter in front of the isolated amplifier improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is high and only a small-value filter capacitor can be used to not limit the signal bandwidth to an unacceptable low value. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal $\Delta \Sigma$ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter

Most voltage-sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor (as shown in 图 9-2) is sufficient to filter the input signal.

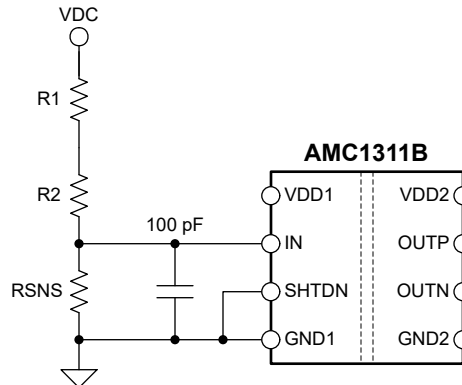


图 9-2. Input Filter

9.2.2.2 Differential to Single-Ended Output Conversion

图 9-3 shows an example of a TLV900x-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With $R1 = R2 = R3 = R4$, the output voltage equals $(V_{OUTP} - V_{OUTN}) + V_{REF}$. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, $R1 = R2 = R3 = R4 = 3.3 \text{ k}\Omega$ and $C1 = C2 = 330 \text{ pF}$ yields good performance.

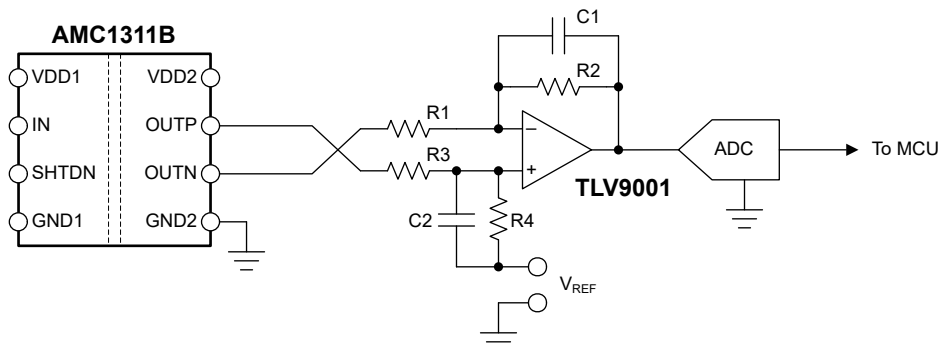


图 9-3. Connecting the AMC1311 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guides, available for download at www.ti.com.

9.2.3 Application Curve

One important aspect of system design is the effective detection of an overvoltage condition to protect switching devices and passive components from damage. To power off the system quickly in the event of an overvoltage condition, a low delay caused by the isolated amplifier is required. 图 9-4 shows the typical full-scale step response of the AMC1311.

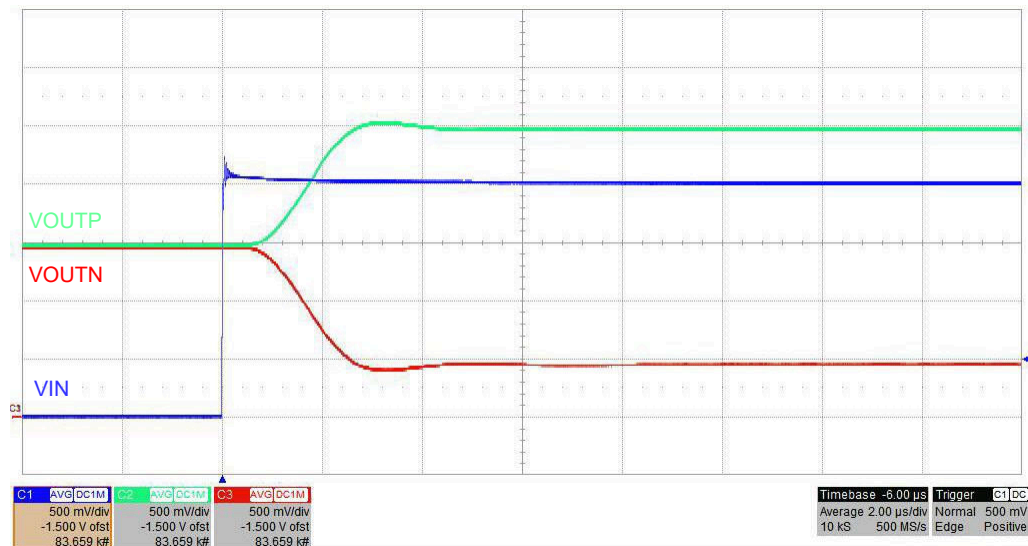


图 9-4. Step Response of the AMC1311

9.3 What To Do and What Not To Do

Do not leave the analog input (IN pin) of the AMC1311 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range, causing the output of the device to be invalid.

Do not connect protection diodes to the input (IN pin) of the AMC1311. Diode leakage current can introduce significant measurement error especially at high temperatures. The input pin is protected against high voltages by its ESD protection circuit and the high impedance of the external resistive divider.

10 Power Supply Recommendations

In a typical application, the high-side (VDD1) of the AMC1311 is powered from an already existing, high-side, ground-referenced, 3.3-V or 5-V power supply in the system. Alternatively, the high-side supply can be generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost solution is based on the push-pull driver [SN6501](#) and a transformer that supports the desired isolation voltage ratings.

The AMC1311 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1- μ F capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1- μ F capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. [图 10-1](#) shows the proper decoupling layout for the AMC1311.

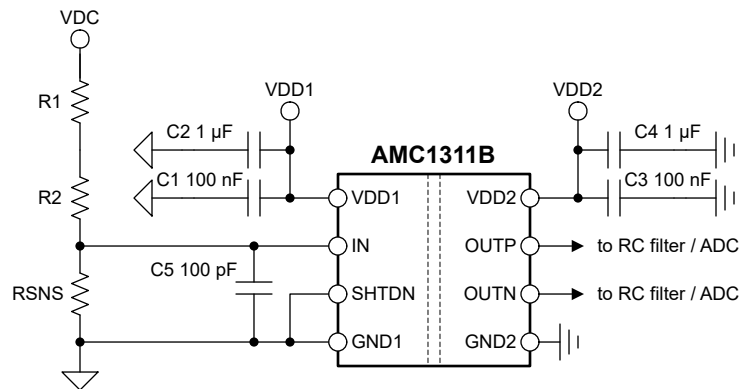


图 10-1. Decoupling of the AMC1311

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

11 Layout

11.1 Layout Guidelines

Figure 11-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1311 supply pins) and placement of the other components required by the device. For best performance, place the sense resistor close to the device input pin (IN).

11.2 Layout Example

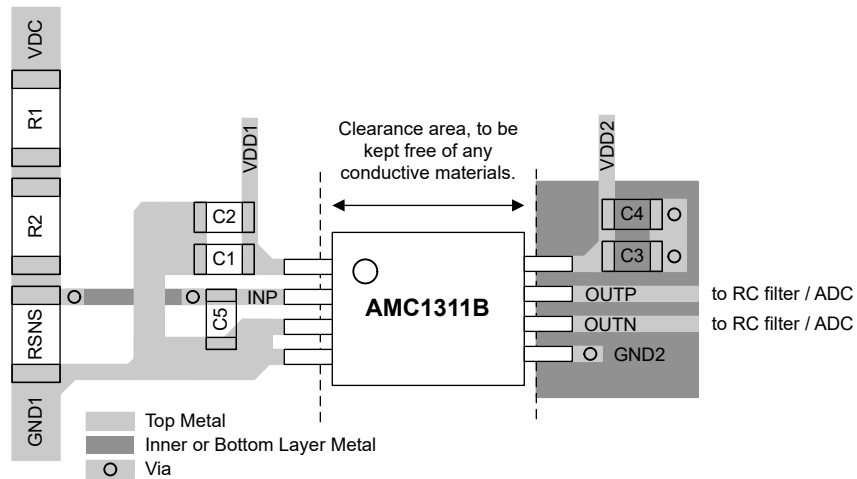


图 11-1. Recommended Layout of the AMC1311

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary application report](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application report](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application report](#)
- Texas Instruments, [TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems data sheet](#)
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [AMC1311EVM Users Guide](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise reference guide](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power reference guide](#)
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator design tool](#)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| AMC1311BDWV | Active | Production | SOIC (DWV) 8 | 64 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWV.A | Active | Production | SOIC (DWV) 8 | 64 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWV.B | Active | Production | SOIC (DWV) 8 | 64 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWVR | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWVR.A | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWVR.B | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWVRG4 | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWVRG4.A | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311BDWVRG4.B | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311B |
| AMC1311DWV | Active | Production | SOIC (DWV) 8 | 64 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1311 |
| AMC1311DWV.B | Active | Production | SOIC (DWV) 8 | 64 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1311 |
| AMC1311DWVR | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1311 |
| AMC1311DWVR.A | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1311 |
| AMC1311DWVR.B | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1311 |
| AMC1311DWVRG4 | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311 |
| AMC1311DWVRG4.A | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311 |
| AMC1311DWVRG4.B | Active | Production | SOIC (DWV) 8 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 125 | 1311 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF AMC1311 :

- Automotive : [AMC1311-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AMC1311BDWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |
| AMC1311BDWVRG4 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |
| AMC1311DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |
| AMC1311DWVRG4 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AMC1311BDWVR | SOIC | DWV | 8 | 1000 | 356.0 | 356.0 | 35.0 |
| AMC1311BDWVRG4 | SOIC | DWV | 8 | 1000 | 356.0 | 356.0 | 35.0 |
| AMC1311DWVR | SOIC | DWV | 8 | 1000 | 356.0 | 356.0 | 35.0 |
| AMC1311DWVRG4 | SOIC | DWV | 8 | 1000 | 356.0 | 356.0 | 35.0 |

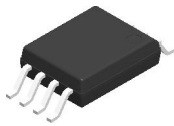
TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| AMC1311BDWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1311BDWV.A | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1311BDWV.B | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1311DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1311DWV.B | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |

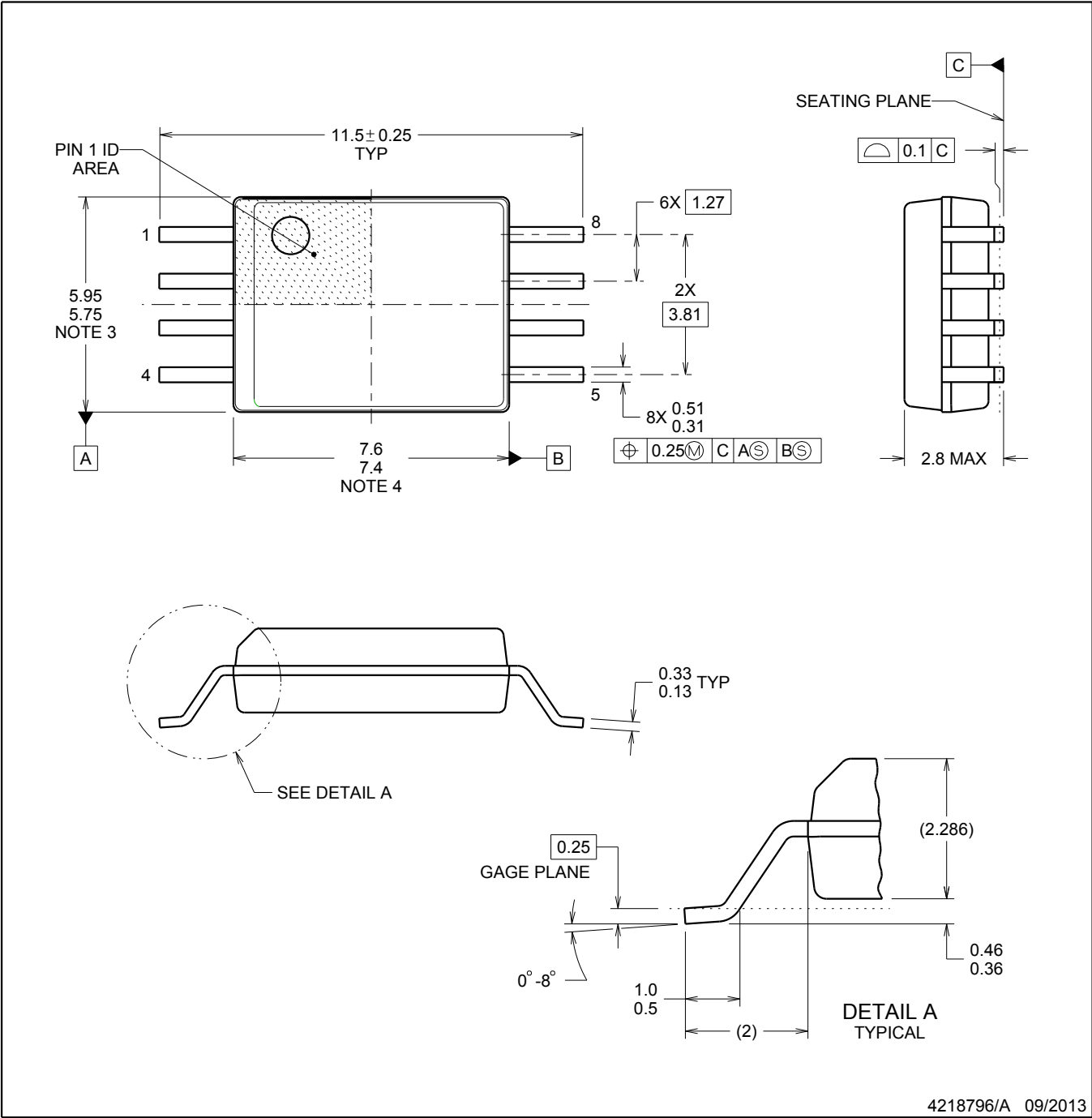
PACKAGE OUTLINE

DWV0008A



SOIC - 2.8 mm max height

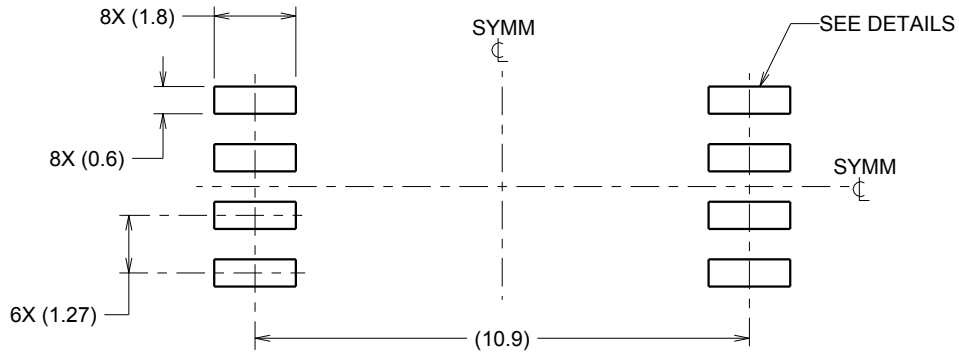
SOIC



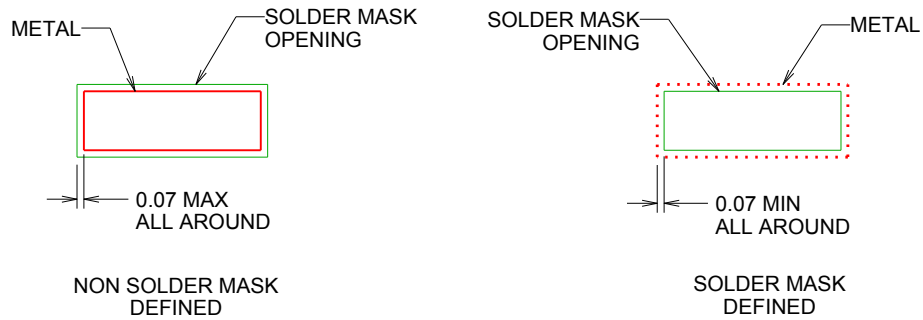
4218796/A 09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

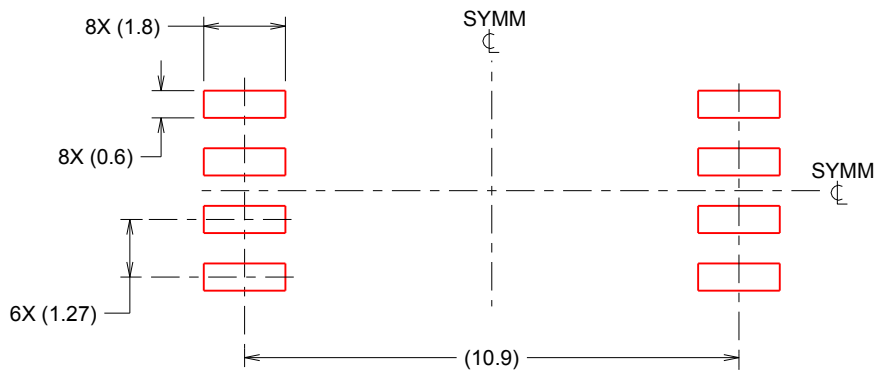


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:6X

4218796/A 09/2013

NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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