3V to 15V Input, Single 15A Step-Down DC/DC Regulator Module

DESCRIPTION

The EZ8626 is a complete single 15A output switching mode step-down DC/DC System-in-Package (SiP) Power Module. Operating over a wide input voltage range of 3V to 15V, the EZ8626 module supports 15A continuouss output ranging from 0.6V to 5.5V set by a single external resistors. Only a few input and output capacitors are needed.

The device supports selectable Pulse Frequency Modulation (PFM) and output soft-start including output pre-biased condition. Its high switching frequency and a quick-response constant on-time current control architecture ensure a very fast transient response to line and load changes.

Fault protection includes accurate over-voltage, over-current and over-temperature protection.

The EZ8626 module is offered in a high density thermally enhanced 5mm×5mm×2.46mm LQFN package with RoHS compliant terminal finish.

FEATURES

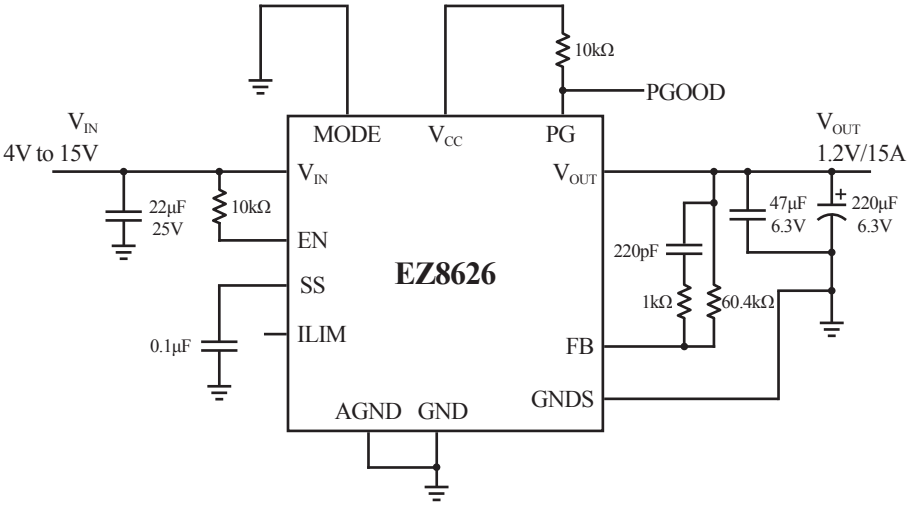
- Complete System-in-Package (SiP) Power Supply in <1cm^2 Solution Size
- Single 15A Output Current
- 3V to 15V Input Voltage Range
- 0.6V to 5.5V Output Voltage Range
- ±1.5% Maximum Total DC Output Error
- Build-in Remote Sensing Amplifier
- Selectable Pulse Frequency Modulation
- Adjustable Switching Frequency
- Constant On-Time Control, Fast Transient Response
- Programmable Current Limit
- Over-voltage, Over-current and Over-temperature Protection
- 5mm×5mm×2.46mm LQFN package

APPLICATIONS

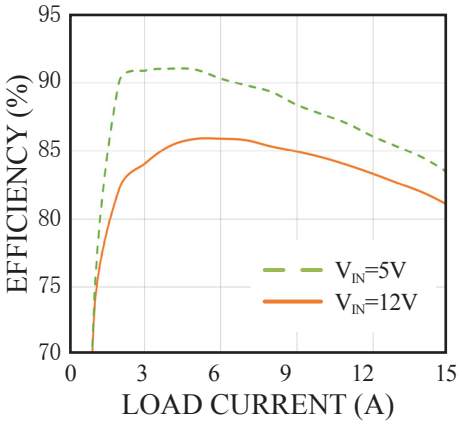
- Point-of-Load Application
- Telecom and Networking Application
- FPGA and ASIC Application

TYPICAL APPLICATION

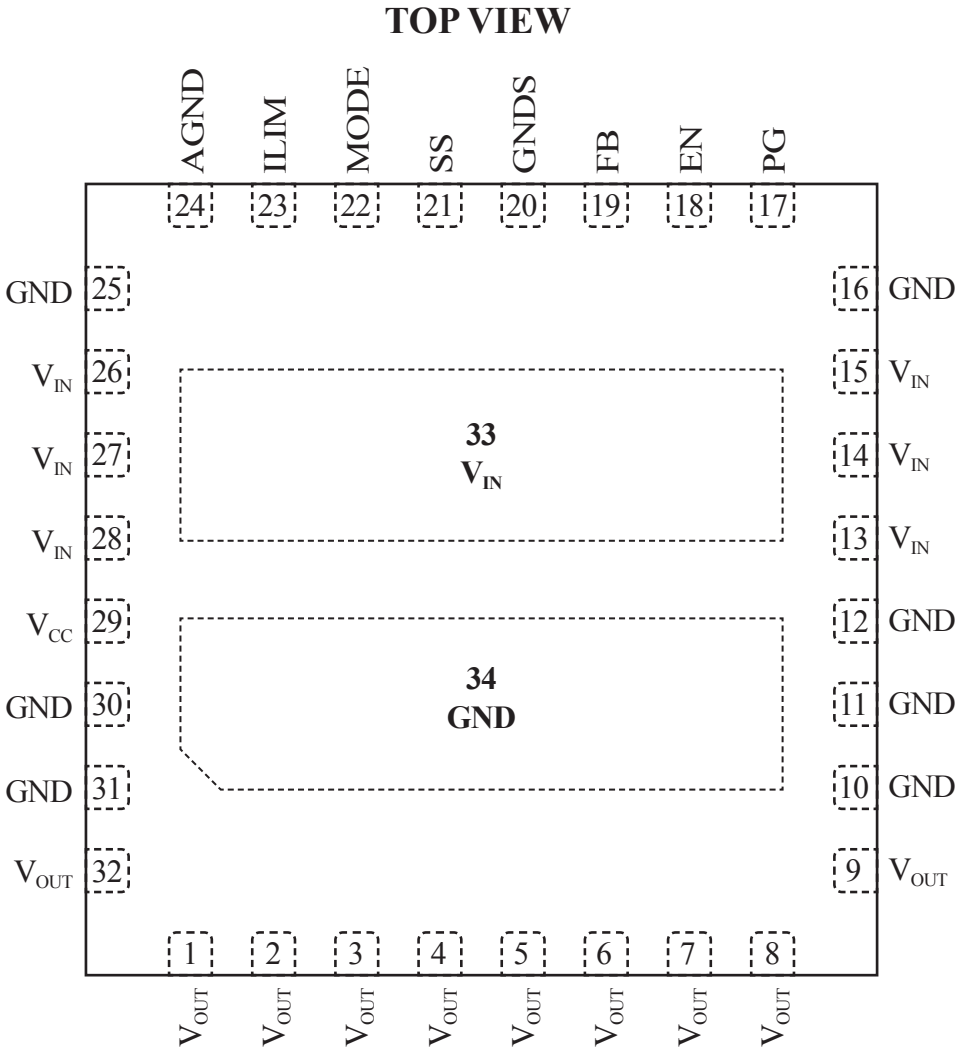
4V to 15V Input, Single 15A Output DC/DC Regulator



Efficiency at 1.2V Output Voltage



PIN CONFIGURATION AND FUNCTIONS



34 LEAD 5mm x 5mm x 2.46mm LQFN Package
T_{JMAX}=125°C, Θ_{JCtop}=TBD°C, $\Theta_{JCbottom}$=TBD°C, Θ_{JA}=TBD°C, Θ_{JB}=TBD°C
Θ value determined per JESD51-12, Weight=0.255 g

PIN#	PIN Name	PIN Description
1-9, 32	V_{OUT}	Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.
10-12, 16, 25, 30-31, 34	GND	Power Ground Pins for Both Input and Output Returns. Must connect all GND pins on the PCB Board.
24	AGND	Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the GND in the application. See layout guidelines in Figure 2.
22	MODE	Force Continuous Current Mode or Pulse Frequency Modulation (PFM) Mode Selection Pin and Operation Frequency Set Pin. Connect a resistor from this pin to AGND to program both mode and frequency. See the Applications Information section.
19	FB	Positive Input Pin of the Internal Differential Sensing Amplifier and Feedback Voltage. This pin is internally connected to GNDS with a 60.4kΩ precision resistor. Differential remote sensing can be achieved by connecting this pin to V_{OUT}+ through a resistor, and GNDS pin to V_{OUT}- at the point of load side. Different output voltages can be programmed by adding a resistor between V_{OUT}+ and FB. See the Applications Information section.
21	SS	Output Voltage Soft-Start input. It has a 46μA pull-up current source. A capacitor from this pin to AGND will set a soft-start ramp rate. See the Applications Information section.
18	EN	Enable Control Pin. A voltage above 1.2V will turn on the module. A voltage below 0.4V on the EN pin will turn off the module. Do not leave this pin floating.
17	PG	Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within -20% to +20% of the regulation point.
29	V_{CC}	Internal 3.3V LDO Regulator Output. The control circuits and internal gate drivers are powered from this voltage. This pin is internally decoupled to GND with a 1μF low ESR ceramic capacitor. No further external decoupling capacitor needed. Connect this pin to V_{IN} when input voltage is below 3.6V.
13-15, 26-28, 33	V_{IN}	Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins. Must connect all V_{IN} pins on the PCB Board.
20	GNDS	Negative Input Pin of the Internal Differential Sensing Amplifier. This pin is internally connected to FB Pin with a 60.4kΩ precision resistor. Connect this pin to the negative of the output at the point of load side to achieve differential remote sensing.
23	ILIM	Valley Current Limit Set Pin. The ILIM pin has 1.2V voltage. A resistor from this pin to AGND sets a current which is compared with bottom FET current with a 10μA/A ratio to trigger current limit protection. See the Applications Information section.

ORDER INFORMATION

PART NUMBER	FINISH	MARKING	PACKAGE TYPE	PACKAGE MATERIAL	MSL	TEMPERATURE RANGE
EZ8626IV#PBF	Au (RoHS)	SF	LQFN	TRAY	3	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS

	MIN	TYP	MAX	UNITS
Terminal Voltage				
V_{IN}	-0.3		16	V
EN	-0.3		VIN+0.3V	V
V_{CC}	-0.3		4	V
FB, GNDS, PG, ILIM, MODE, SS	-0.3		V_{CC}	V
Temperatures				
Internal Operating Temperature Range	-40		125	°C
Storage Temperature Range	-55		150	°C
Peak Solder Reflow Package Body Temperature		260		°C
ESD Rating				
HBM (Human Body Model)	1.5			kV
CDM (Charged Device Model)	1			kV

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ELECTRICAL CHARACTERISTICS

The Y denotes the specifications which apply over full internal operating temperature range (Note 1), otherwise specifications are at T_A = 25°C, V_{IN} = 12V and V_{EN}= 5V per the typical application in Figure 3 unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	FTR
V_{IN}	Input DC Voltage		3.6		15	V	Y
		V_{IN} and V_{CC} Connect Together	3		3.6	V	Y
$V_{OUT(RANGE)}$	Output Voltage Range	V_{IN} = 3V to 15V	0.6		5.5	V	Y
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22uF C_{OUT} = 47µF Ceramic+220µF POSCAP R_{FB} = 90.6k, MODE = GND V_{IN} = 3.6V to 15V, I_{OUT} = 0A to 15A	1.477	1.50	1.523	V	Y
Input Specifications							
V_{EN}	EN Pin On Threshold	V_{EN} Rising	1.18	1.23	1.28	V	
V_{EN_HYS}	EN Pin On Hysteresis			0.2		V	
UVLO	Undervoltage Lockout	V_{IN} Rising	2.6	2.75	2.9	V	

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	FTR
UVLO_HYS	UVLO Hysteresis			0.2		V	
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0 A PFM Mode Switching Continuous Shutdown, V_{EN} = 0, V_{IN} = 12V		710 45 2		µA mA µA	
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 15A		2.3		A	
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V	0		15	A	
$\frac{\Delta V_{OUT\,(Line)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 3.6V to 15V I_{OUT} = 0A		0.05	0.15	%/V	Y
$\frac{\Delta V_{OUT\,(Load)}}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 15A		0.5	0.75	%	Y
$V_{OUT(AC)}$	Output Ripple Voltage	C_{OUT} = 47µF Ceramic + 220µF POSCAP V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A		20		mV	
t_{START}	Turn-On Time	C_{OUT} = 47µF Ceramic + 220µF POSCAP V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A SS = 0.01µF		1		ms	
Control Specification							
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	0.594	0.600	0.606	V	Y
I_{FB}	Current at FB Pin	(Note 3)			-50	nA	
I_{SS}	SS Pin Soft-Start Pull-Up Current	SS = 0V		46		µA	
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)		60		ns	
R_{FB_BOT}	Resistor Between FB and GNDS Pin		60.05	60.40	60.75	kΩ	
V_{PG}	PG Trip Level	FB With Respect to Set Output FB Ramping Negative FB Ramping Positive	 -23 10	 -20 20	 -12 30	 % %	
I_{PG}	PG Leakage Current	V_{PG} = 3.3V		3	5	µA	
V_{PG_LOW}	PG Voltage Low	I_{PG} = 2mA		0.03	0.3	V	
t_{PG}	PG Delay	PG Rising PG Falling		0.8 20		ms µs	
Internal Linear Regulator							
V_{CC}	V_{CC} Voltage	4V ≤ V_{IN} ≤15V	3.15	3.3	3.45	V	
V_{CC_REG}	V_{CC} Load Regulation	V_{INT} = 0 to 25mA		1.4		%	
Frequency Oscillator and PLL							
f_{NOM}	Nominal Frequency	R_{MODE}=0Ω	510	600	690	kHz	
		R_{MODE}=30.1kΩ	690	800	910	kHz	
		R_{MODE}=60.4kΩ	900	1000	1100	kHz	

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	FTR
Protection							
OV	Over Voltage Threshold	V_{FB}/V_{REF}	110	120	130	%	
UV	Under Voltage Threshold	V_{FB}/V_{REF}	45	50	55	%	
V_{ILIM}	ILIM pin voltage		1.15	1.2	1.25	V	
ILIM	Current Limit	Peak Valley		28 15		A A	
T_{SD}	Thermal Shutdown Temperature	T_J Rising		160		°C	
T_{HYS}	Thermal Shutdown Hysteresis			30		°C	

Note 1: The EZ8626 is tested under pulsed load conditions such that $T_J \approx T_A$. The EZ8626I is guaranteed over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 2:EZ8626 device is designed to operate from 600kHz to 1000kHz

Note 3: These parameters are tested at wafer sort.

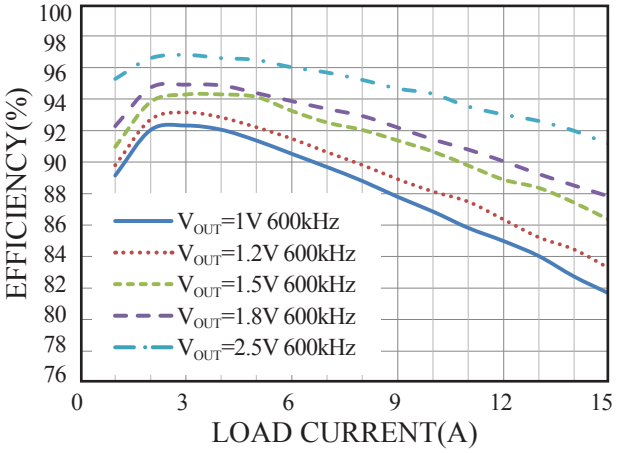
Note 4:FTR means Full Temperature Range.

REVISION HISTORY

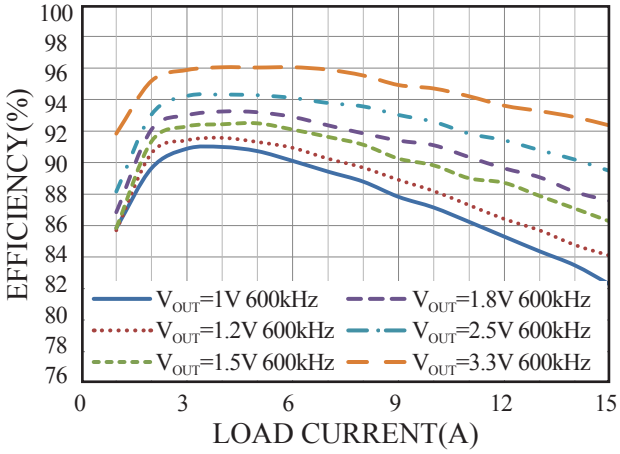
REV.	DATE	CHANGES
C	Mar 2023	Fix typos
B	Jun 2022	Update to 15A output
A	Apr 2022	Initial Release

ELECTRICAL CHARACTERISTICS

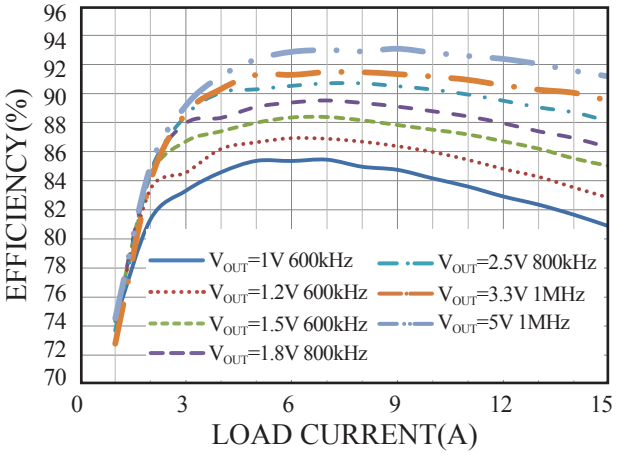
Efficiency vs Load Current From 3.3V Input



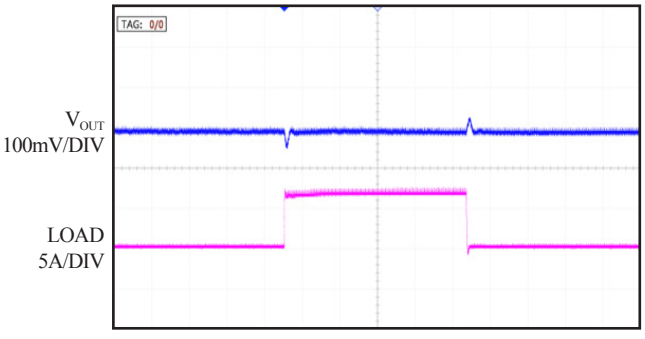
Efficiency vs Load Current From 5V Input



Efficiency vs Load Current From 12V Input

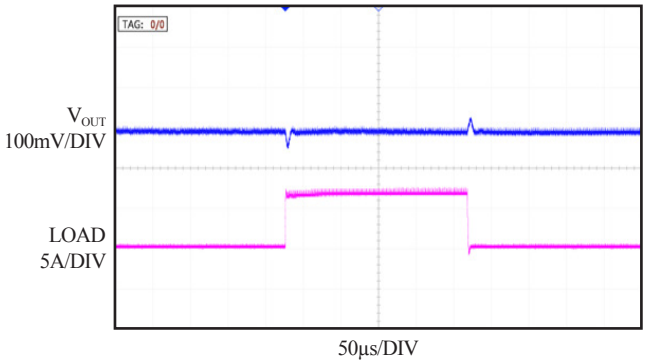


1.0V Output Transient Response



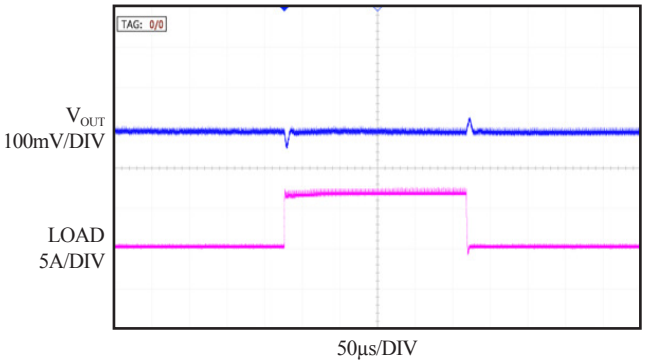
VIN=12V, VOUT=1V, 7.5A LOAD STEP
COUT= 47μFx1 + 100μFx2 CERAMIC CAP

1.5V Output Transient Response



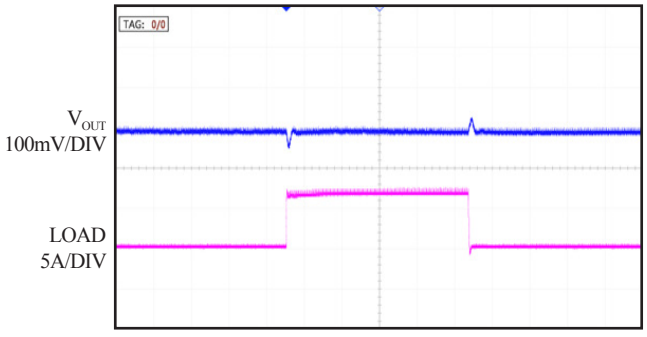
VIN=12V, VOUT=1.5V, 7.5A LOAD STEP
COUT= 47μFx1 + 100μFx2 CERAMIC CAP

2.5V Output Transient Response



VIN=12V, VOUT=2.5V, 7.5A LOAD STEP
COUT= 47μFx1 + 100μFx2 CERAMIC CAP

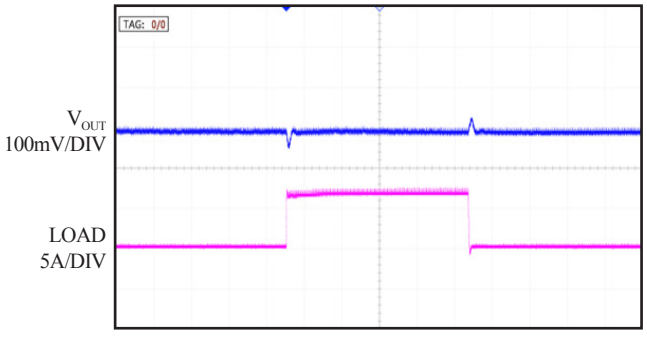
3.3V Output Transient Response



50µs/DIV

V_{IN}=12V, V_{OUT}=3.3V, 7.5A LOAD STEP
COUT= 47µFx1 + 100µFx2 CERAMIC CAP

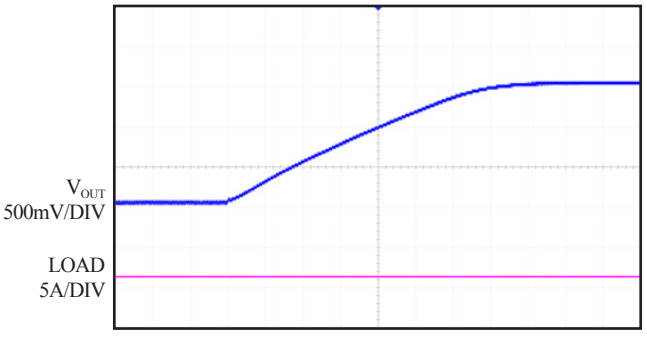
5V Output Transient Response



50µs/DIV

V_{IN}=12V, V_{OUT}=5V, 7.5A LOAD STEP
COUT= 47µFx1 + 100µFx2 CERAMIC CAP

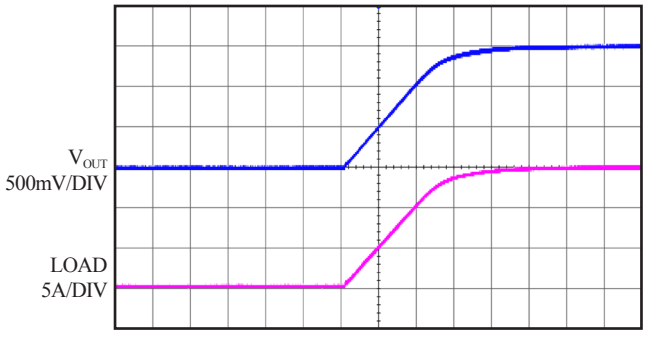
Start-Up with No Load Current



200µs/DIV

V_{IN}=12V, V_{OUT}=1.5V, USE EN PIN TO CONTROL START-UP
IOUT=0A, COUT= 47µFx1 + 100µFx2 CERAMIC CAP
SOFT-START CAPACITOR=0.1µF

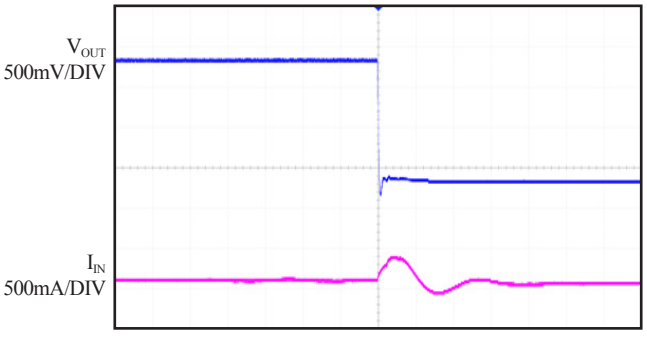
Start-Up with 15A Load Current



500µs/DIV

V_{IN}=12V, V_{OUT}=1.5V, USE EN PIN TO CONTROL START-UP
IOUT=15A, COUT= 47µFx1 + 100µFx2 CERAMIC CAP
SOFT-START CAPACITOR=0.1µF

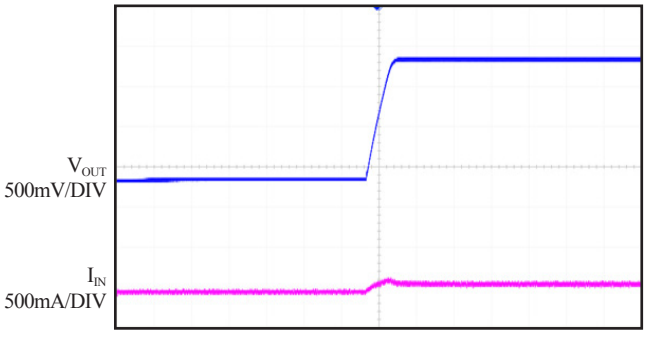
Short Circuit Protection



50µs/DIV

V_{IN}=12V, V_{OUT}=1.5V, IOUT=0A
COUT= 47µFx1 + 100µFx2 CERAMIC CAP
SOFT-START CAPACITOR=0.1µF

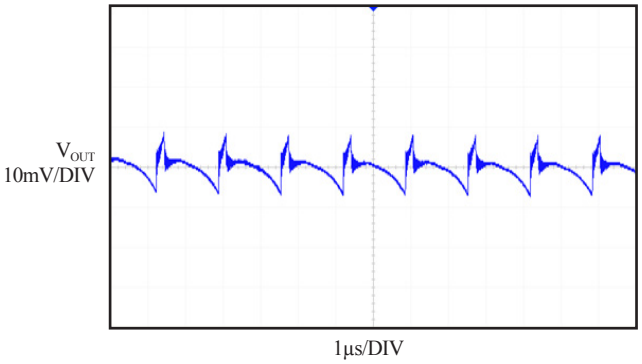
Short Circuit Protection Recovery



2ms/DIV

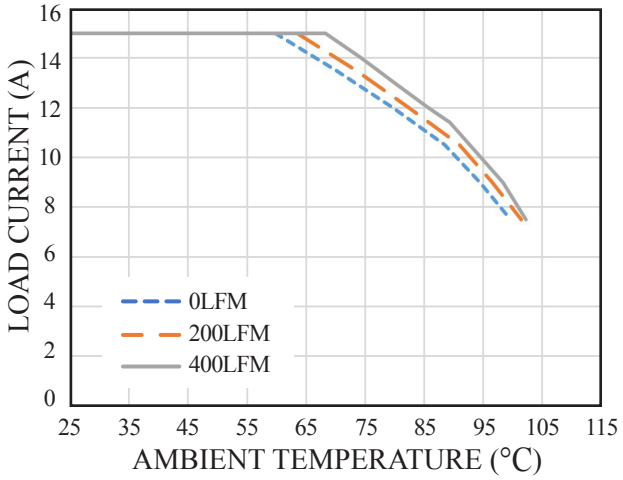
V_{IN}=12V, V_{OUT}=1.5V, IOUT=0A
COUT= 47µFx1 + 100µFx2 CERAMIC CAP
SOFT-START CAPACITOR=0.1µF

Output Steady-State Ripple

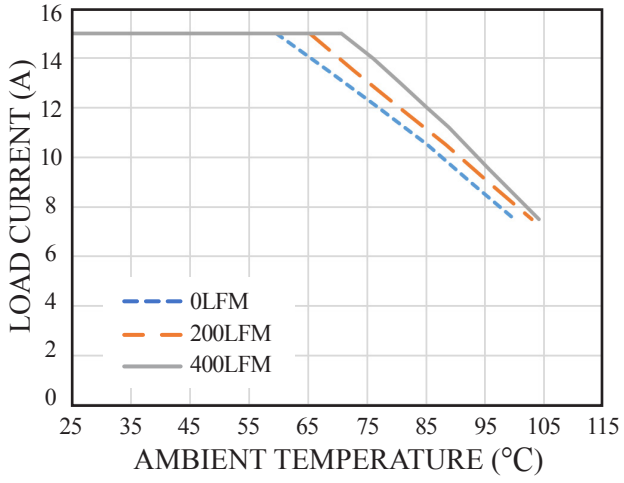


V_{IN}=12V, V_{OUT}=1.5V, IOUT=0A
COUT= 47μFx1 + 100μFx2 CERAMIC CAP

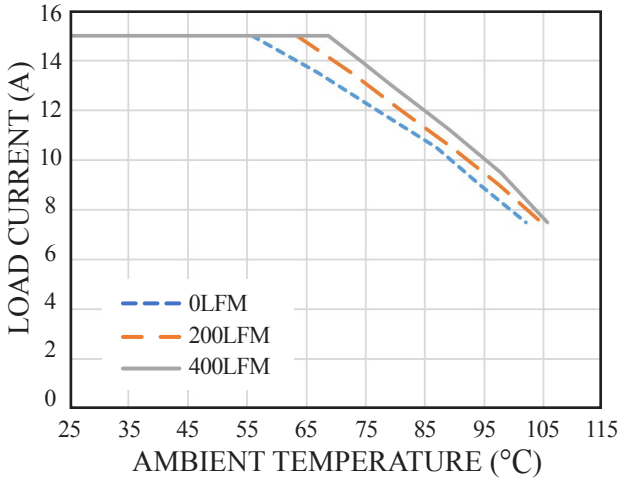
Derating Curve: V_{IN}=3.3V, V_{OUT}=1V, F_{SW}=600kHz



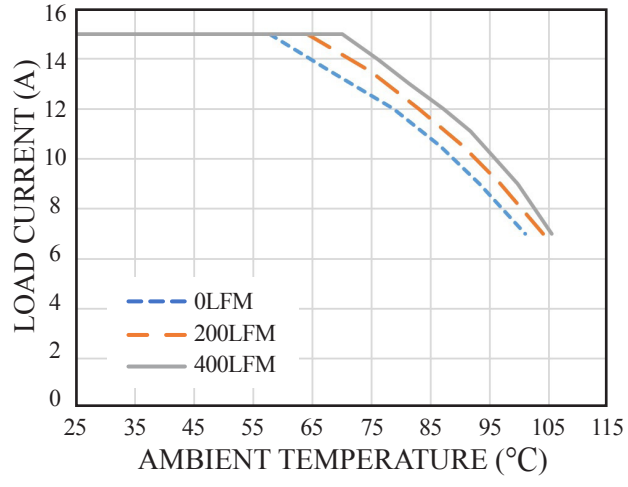
Derating Curve: V_{IN}=3.3V, V_{OUT}=1.2V, F_{SW}=600kHz



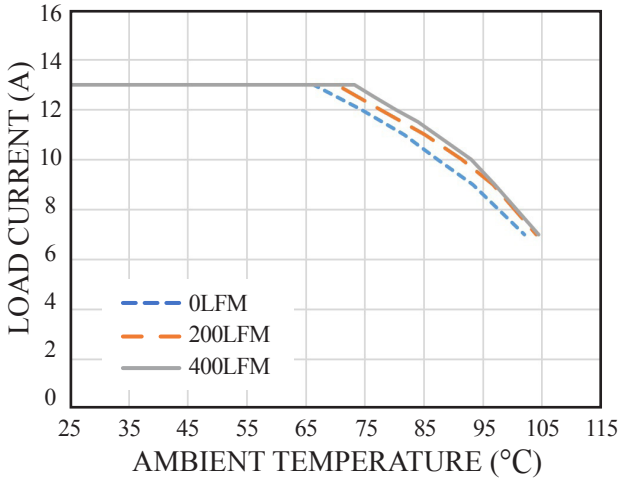
Derating Curve: V_{IN}=3.3V, V_{OUT}=1.5V, F_{SW}=600kHz



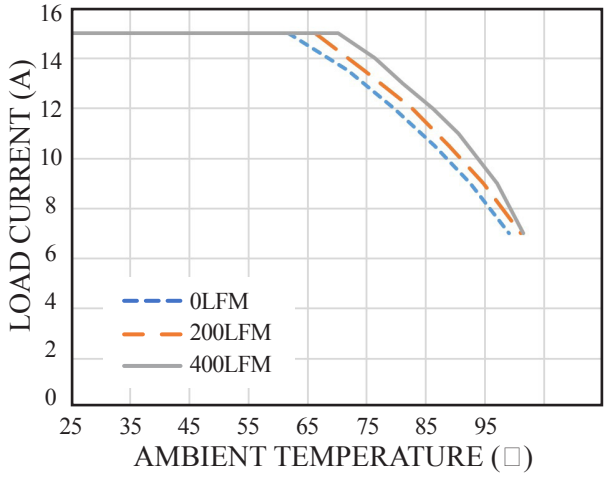
Derating Curve: V_{IN}=3.3V, V_{OUT}=1.8V, F_{SW}=600kHz



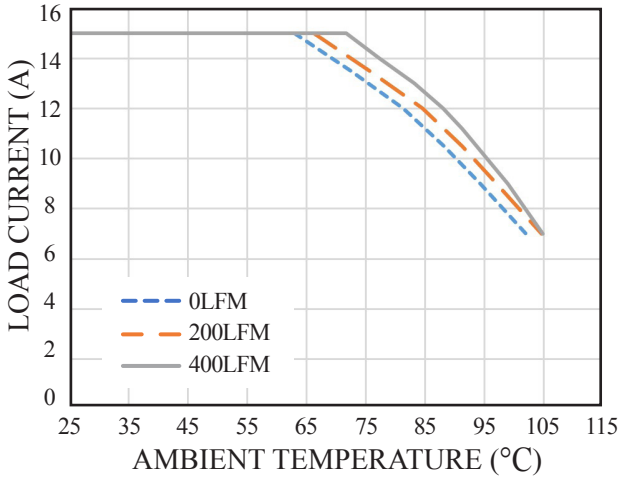
Derating Curve: V_{IN}=3.3V, V_{OUT}=2.5V, F_{SW}=600kHz



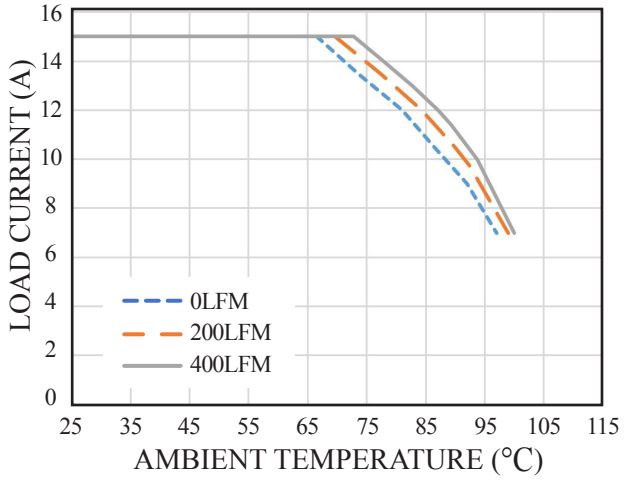
Derating Curve: V_{IN}=5V, V_{OUT}=1V, F_{SW}=600kHz



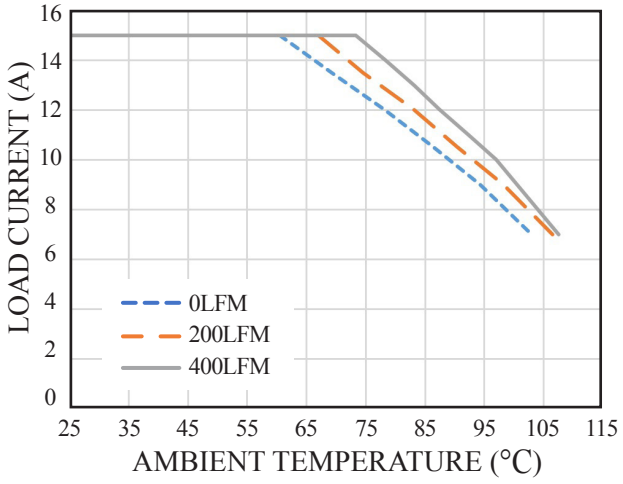
Derating Curve: V_{IN}=5V, V_{OUT}=1.2V, F_{SW}=600kHz



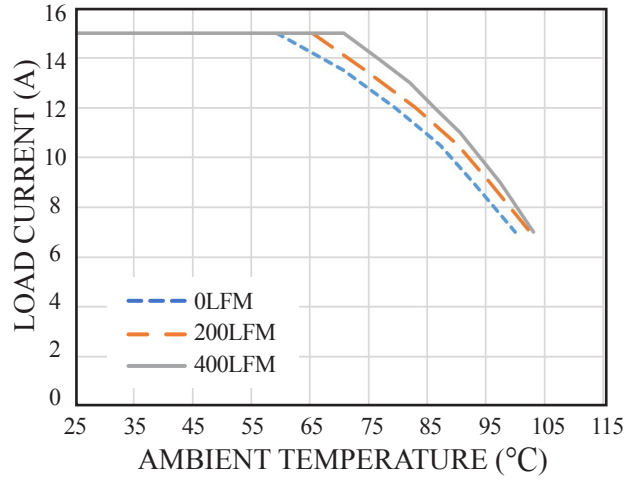
Derating Curve: V_{IN}=5V, V_{OUT}=1.5V, F_{SW}=600kHz



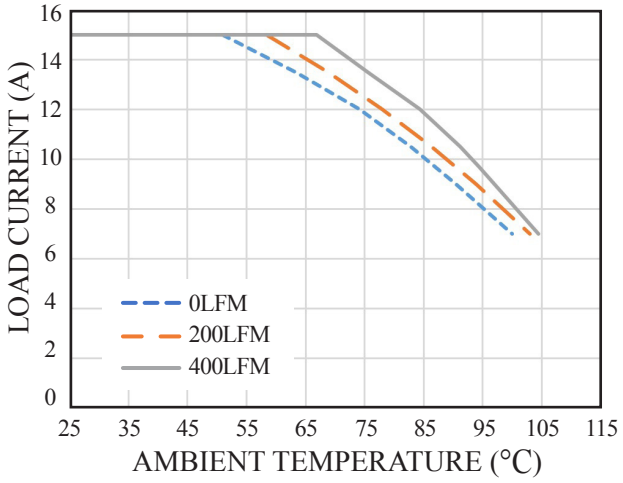
Derating Curve: V_{IN}=5V, V_{OUT}=1.8V, F_{SW}=600kHz



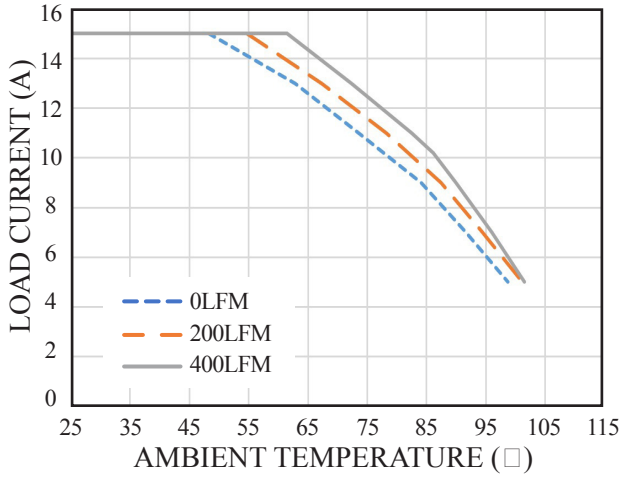
Derating Curve: V_{IN}=5V, V_{OUT}=2.5V, F_{SW}=600kHz



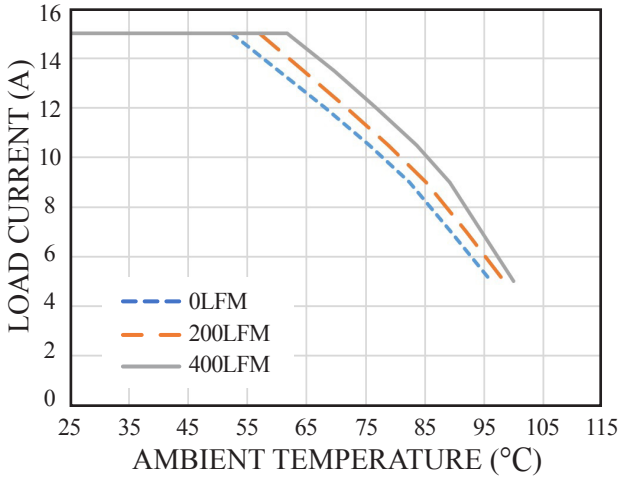
Derating Curve: V_{IN}=5V, V_{OUT}=3.3V, F_{SW}=600kHz



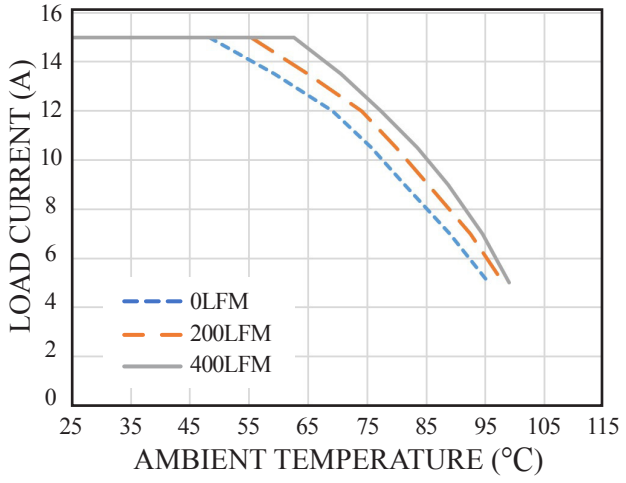
Derating Curve: V_{IN}=12V, V_{OUT}=1V, F_{SW}=600kHz



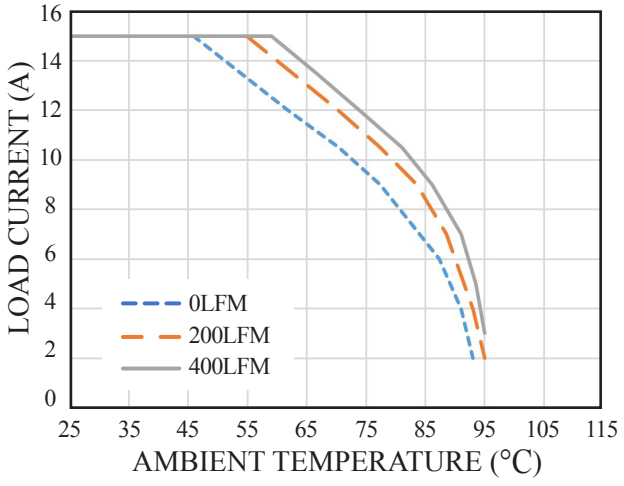
Derating Curve: V_{IN}=12V, V_{OUT}=1.2V, F_{SW}=600kHz



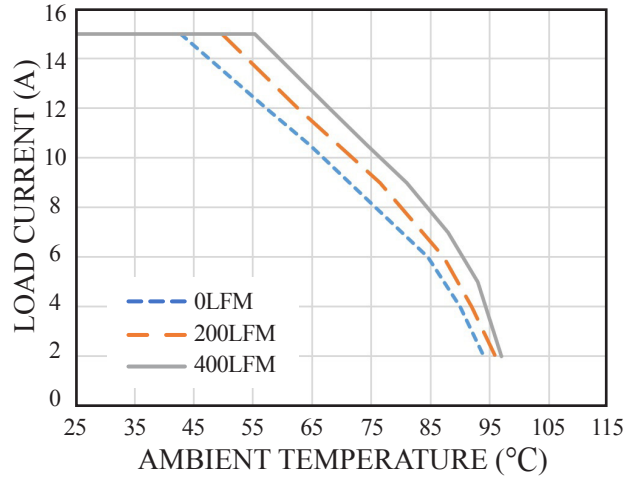
Derating Curve: V_{IN}=12V, V_{OUT}=1.5V, F_{SW}=600kHz



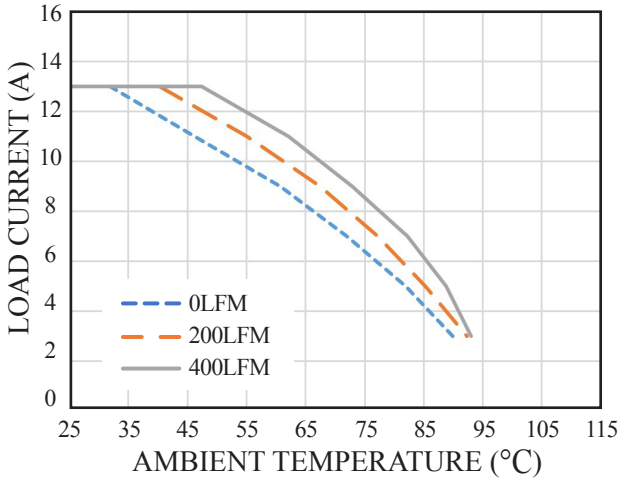
Derating Curve: V_{IN}=12V, V_{OUT}=1.8V, F_{SW}=800kHz



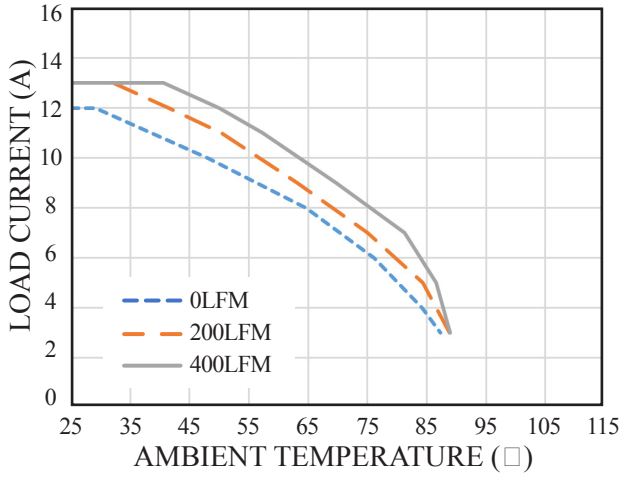
Derating Curve: V_{IN}=12V, V_{OUT}=2.5V, F_{SW}=800kHz



Derating Curve: V_{IN}=12V, V_{OUT}=3.3V, F_{SW}=1MHz



Derating Curve: V_{IN}=12V, V_{OUT}=5V, F_{SW}=1MHz



BLOCK DIAGRAM

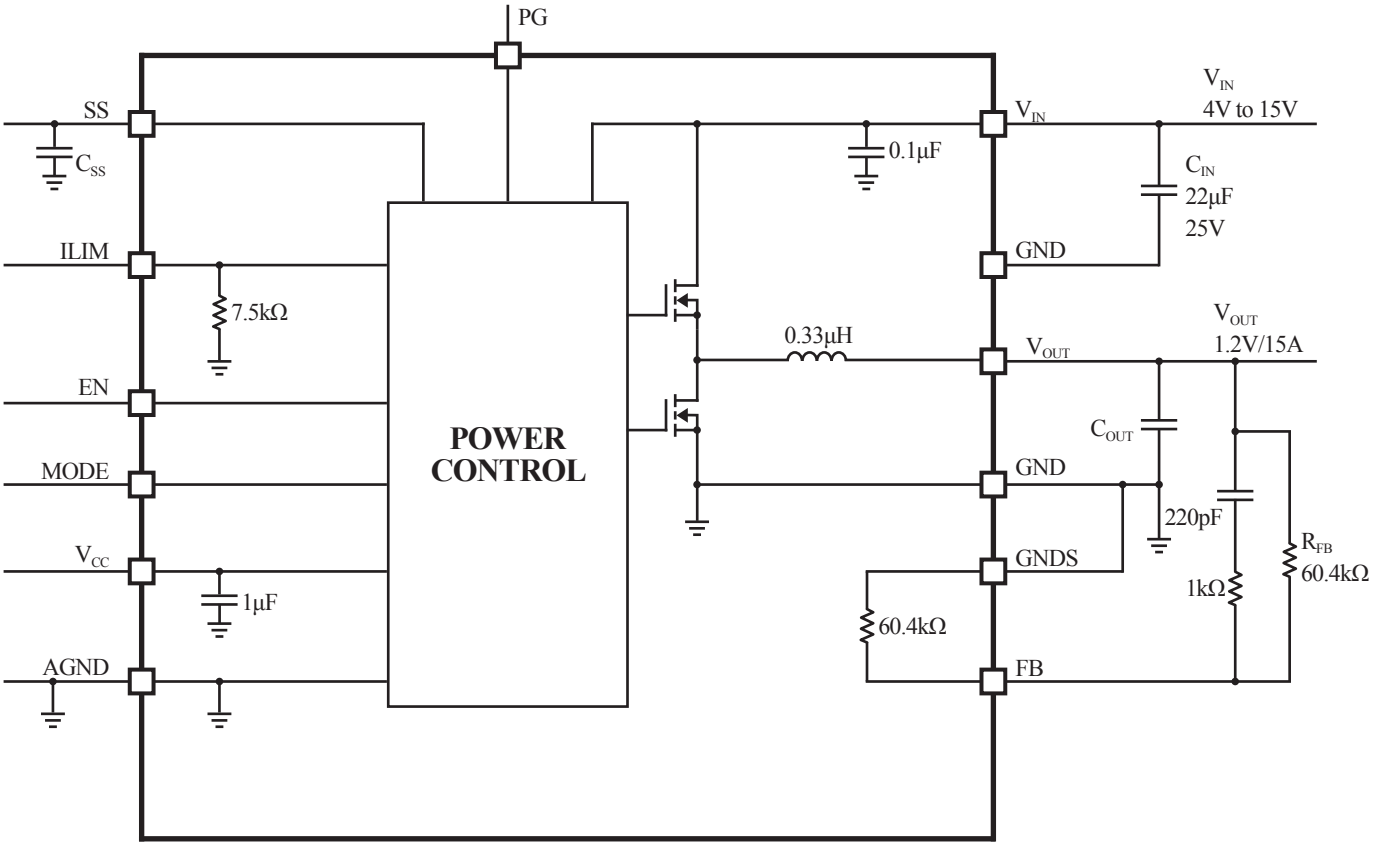


Figure 1 Simplified EZ8626 Internal Function Block Diagram

OPERATION

POWER MODULE DESCRIPTION

The EZ8626 SiP Power Module is a high-performance single output stand-alone non-isolated switching mode DC/DC power supply. It can provide a single 15A DC output with few external input and output capacitors. This module provides a precisely regulated output voltage programmable via an external resistor from 0.6V to 5.5V over a 3V to 15V input voltage range. The typical application schematic is shown in Figure 3.

The EZ8626 SiP Power Module has an integrated constant on-time (COT) regulator and built-in power MOSFET, power inductor, and other supporting components. The typical switching frequency can be programmed from 600kHz to 1MHz. See the Applications Information section.

During a load transient event, with the help of COT control architecture, the EZ8626 SiP Power Module can turn on its high-side power switch immediately to achieve a very good transient performance with sufficient stability margins over a wide range of output capacitors, even with all ceramic output capacitors.

Pulling EN pin below 0.4V forces the regulator into a shutdown state. The SS pin is used for programming the output voltage soft-start ramp during the start-up. See the Application Information section.

High efficiency at light loads can be accomplished with selectable Pulse Frequency Modulation Mode (PFM) operation by using the MODE pin.

A cycle-by-cycle valley current limit can be programmed by ILIM pin.

APPLICATIONS INFORMATION

The typical EZ8626 application circuit is shown in Figure 3. External component selection is primarily determined by the maximum load current and output voltage.

OUTPUT VOLTAGE PROGRAMMING

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k accuracy internal feedback resistor connects from the FB pin to the GNDS pin.

Adding a resistor R_{FB} from V_{OUT} to FB programs the output voltage as following equation:

$$V_{OUT} = 0.6V \times \frac{R_{FB} + 60.4k\Omega}{60.4k\Omega}$$

Table 1 FB Resistor Table vs Various Output Voltages

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5
R_{FB}(kΩ)	0	40.2	60.4	90.6	121	191	274	442

INPUT CAPACITORS

The EZ8626 SiP Power Module should be connected to a low AC-impedance DC source. Also input ceramic capacitors are needed for the RMS input ripple current rating. A typical 22µF ceramic capacitor is a good choice with RMS ripple current ratings of ~2A each.

A 47uF to 100µF aluminum electrolytic bulk capacitor can be added only if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \times \sqrt{D \times (1 - D)}$$

η% is the estimated efficiency of the power module.

OUTPUT CAPACITORS

The EZ8626 is designed for low output voltage ripple noise. To meet the output voltage ripple and transient requirements, The output capacitor C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or even all ceramic capacitors.

The typical output capacitance range is from 100µF to 220µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required.

FREQUENCY SELECTION

The EZ8626 is optimized over a range of frequencies depending on input and output voltage to improve power conversion efficiency. It is recommended to operate the lower output voltages or lower duty cycle conversions at lower frequencies to improve efficiency by lowering power MOSFET switching losses. Higher output voltages or higher duty cycle conversions can be operated at higher frequencies to limit inductor ripple current. The efficiency graphs will show an operating frequency chosen for that condition. See Table 2 for optimized frequency for various output voltages.

The EZ8626 switching frequency can be programmed to 600kHz, 800kHz and 1MHz by connecting an external resistor from the MODE pin to AGND. See Table 2 for different resistor value.

Table 2 Optimized Frequency vs Input and Output Voltage

V_{IN}(V)	V_{OUT}(V)	F_{sw}	MODE	R_{MODE}
3.3	ALL	600kHz	FCCM	GND
			PFM	VCC
5	ALL	600kHz	FCCM	GND
			PFM	VCC
12	0.6~1.5	600kHz	FCCM	GND
			PFM	VCC
	1.8~2.5	800kHz	FCCM	30kΩ
			PFM	240kΩ
	3.3~5.5	1MHz	FCCM	60kΩ
			PFM	120kΩ

PFM OPERATION

In applications where low output ripple and high efficiency at intermediate currents are desired, Pulse Frequency Modulation (PFM) should be used. In PFM operation, the low side synchronous rectifier MOSFET turns off to prevent the inductor current go negative during the light load condition. If the load current is further reduced, the

control circuit will start to reduce switching frequency to further enhance efficiency. The switching frequency could be lower than audible frequency area under deep light load condition.
PFM operation can be enabled by selecting different MODE pin resistor. See Table 2 for different resistor value.

FCCM OPERATION

In applications where fixed frequency operation is more critical than light load efficiency, and where the lowest output ripple is desired, Forced Continuous Current Mode (FCCM) operation should be used. FCCM operation can be enabled by selecting different MODE pin resistor. See Table 2 for different resistor value.

SOFT-START

The EZ8626 incorporates an internal soft-start to reduce the voltage and current stress during the start-up. The internal soft-start is set to approximately 1ms.
The soft-start time can be further increased by connecting an external capacitor from the SS pin to AGND. An internal 46μA current source will charge up the external soft-start capacitor towards V_{CC} voltage. The external soft-start time can be calculated as:

$$t_{SS}(\text{ms}) = 0.6\text{V} \times \frac{C_{SS}(\text{nF})}{46\mu A}$$

where C_{SS} is the capacitance on the SS pin.
The control circuit will take the longer of internal or external soft-start time.

EN PIN ENABLE

The EN pin has an enable threshold of 1.28V maximum, typically 1.23V with 200mV of hysteresis. When EN voltage rises to around 0.8V, V_{CC} becomes active. Further increase EN voltage to 1.23V will enable the switching action and normal device operation. When EN voltage is lower than 0.4V, the V_{CC} will be shut down, reducing the input current to <5 μA.
A pull-up resistor between 1kΩ and 1MΩ should be used if EN is pulled high using V_{IN} directly.

POWER GOOD

The PG pin is open drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±20% window around the regulation point with certain delay. A resistor can be pulled up to a particular supply voltage no greater than 4V maximum for monitoring.

OVER-CURRENT PROTECTION

The EZ8626 SiP Power Module has a cycle-by-cycle valley current mode over current protection (OCP) in a short circuit. The top MOSFET will keep off until the current returns back to safe level. The default valley current limit is set to around 15A to guarantee a DC output current higher than 15A.
The valley current limit point can be programmed by ILIM pin.
An external resistor between ILIM pin and AGND pin could increase this valley current limit point to a higher value using the following equation.

$$I_{lim\_valley} = \frac{1.2V}{10\mu\text{A/A} \times \frac{7.5k \times R_{ILIM}}{7.5k + R_{ILIM}}\Omega}$$

An external resistor between V_{CC} pin and ILIM pin could reduce this valley current limit to a lower value using the following equation:

$$I_{lim\_valley} = \frac{\frac{1.2V}{7.5k} - \frac{3.3V - 1.2V}{R_{ILIM}}}{10\mu\text{A/A}}$$

The OCP limits the inductor current but the device does not latch off. Under an over current condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall off. Eventually,it will end up with crossing the under voltage protection (UVP) threshold and the device will enter hic-cup protection mode.

OUTPUT UNDER VOLTAGE PROTECTION (UVP)

If the output voltage is less than 50% of the set voltage point for approximately 20μs occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will

enter into hic-cup protection mode. The minimum hic-cup on time is 3ms, and the minimum hic-cup off time is 12ms. If the output fault conditions are removed, the device will go back to normal operation in the nearest hic-cup on time.

OVER TEMPERATURE PROTECTION (OTP)

The EZ8626 incorporates an over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The device will shut down when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 30°C, the device will resume normal operation after a complete soft-start cycle.

V_{CC} LINEAR REGULATOR

The EZ8626 SiP Power Module has an internal 3.3V low dropout regulator that is derived from the input voltage. This regulator is used to power the control circuitry and the power MOSFET drivers. This linear regulator is internally decoupled with a 1μF ceramic capacitor. No further decoupling capacitor is required externally.

OUTPUT DISCHARGE FUNCTION

The EZ8626 discharges the output voltage when the converter shut down from V_{IN} or EN, or thermal shutdown, so that output voltage can be discharged in a minimal time, even load current is zero. The discharging FET which in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shut down logic is triggered. The output discharge FET $R_{DS(ON)}$ is typically 120Ω under room temperature. Note that the discharge FET is not active beyond these shutdown conditions.

PRE-BIASED OUTPUT START-UP

In the application that require the power supply to start up with a pre-bias on the output capacitors, the EZ8626 module can safely power up into a pre-biased output without discharging it.

The EZ8626 accomplishes this by disabling both the top and bottom MOSFETs until the SS pin voltage and the internal soft-start voltage are above the FB pin voltage.

STABILITY COMPENSATION

The EZ8626 module has already been internally compensated for all output voltages.

LAYOUT CHECKLIST/EXAMPLE

The high integration of EZ8626 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated AGND ground copper area for components connected to signal pins. Connect the AGND to GND underneath the unit.
- Bring out test points on the signal pins for monitoring.

Figure 2 gives a good example of the recommended PCB layout.

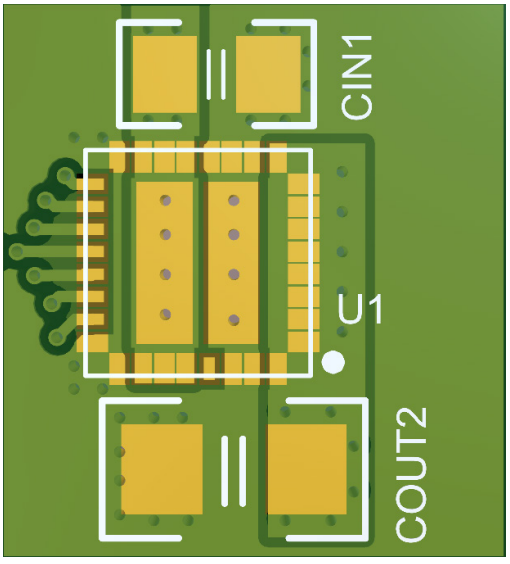


Figure 2 Recommended PCB Layout

TYPICAL APPLICATIONS

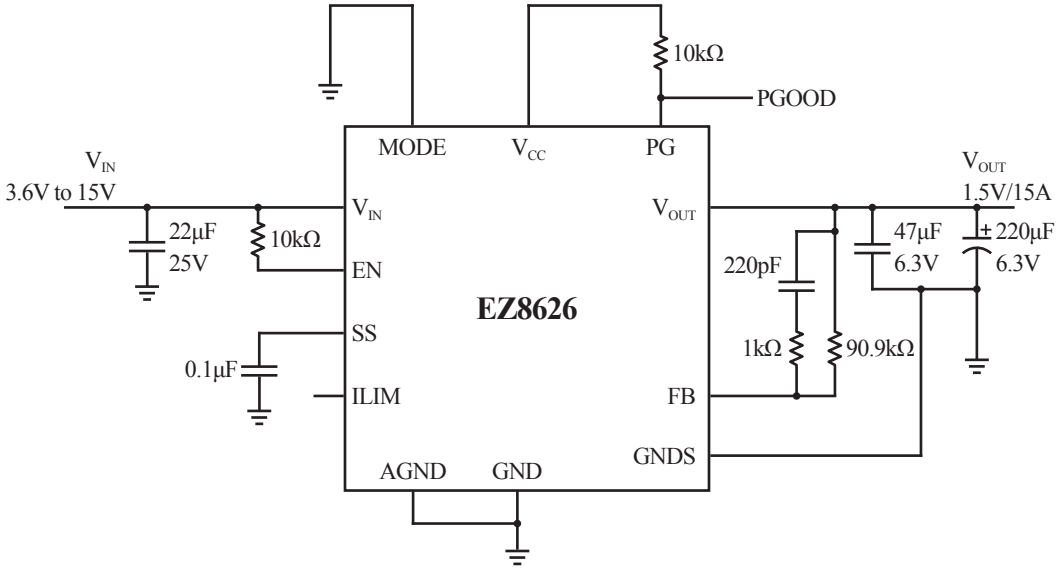


Figure 3 Typical 3.6V to 15V Input, 1.5V at 15A Output Design with 600kHz Frequency

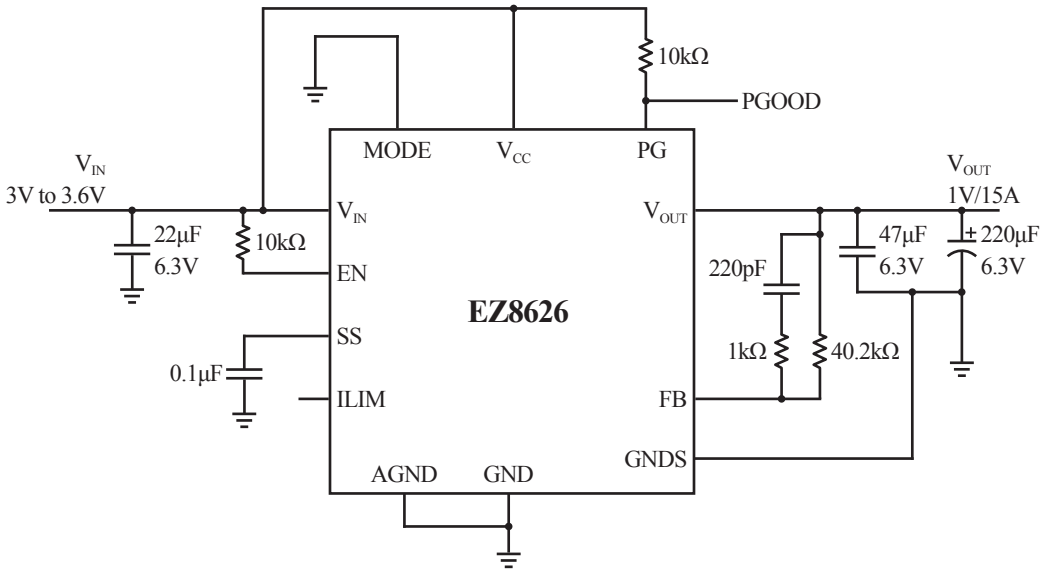


Figure 4 3V to 3.6V Input, 1.0V at 15A Output Design with 600kHz Frequency

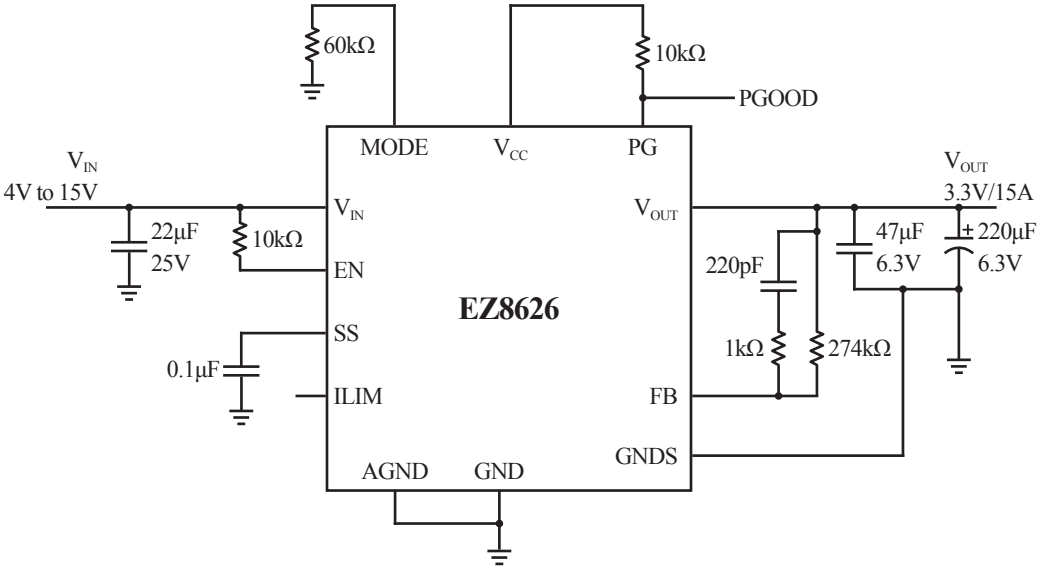
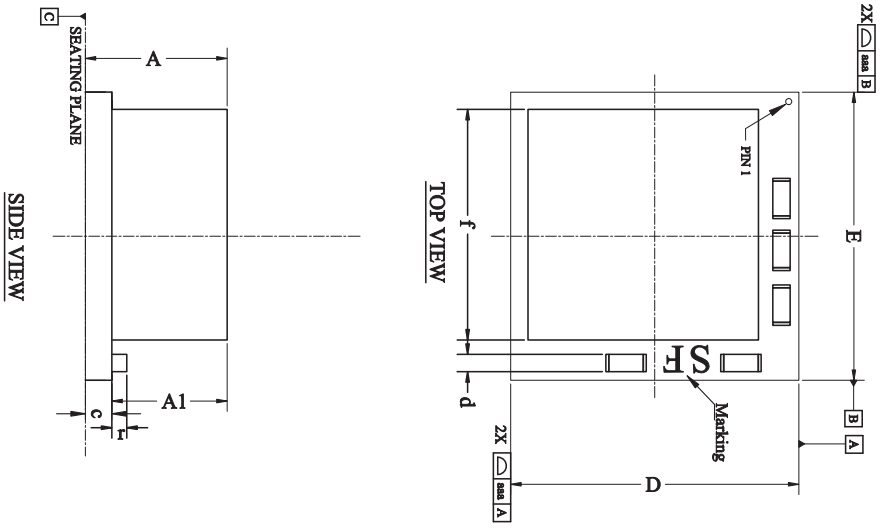


Figure 5 4V to 15V Input, 3.3V at 15A Output Design with 1MHz Frequency

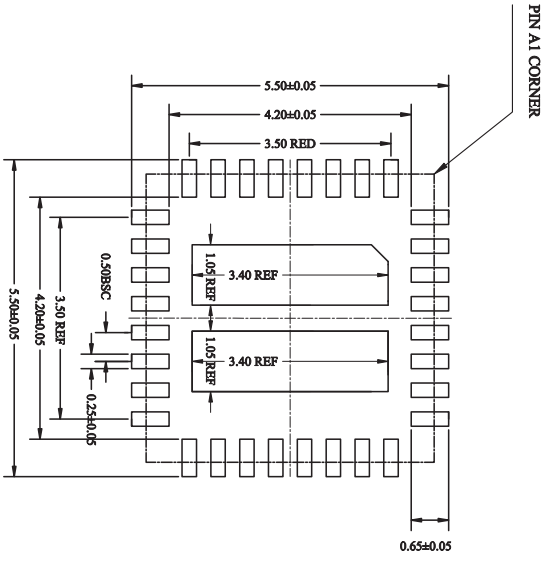
PACKAGING OUTLINE DRAWING

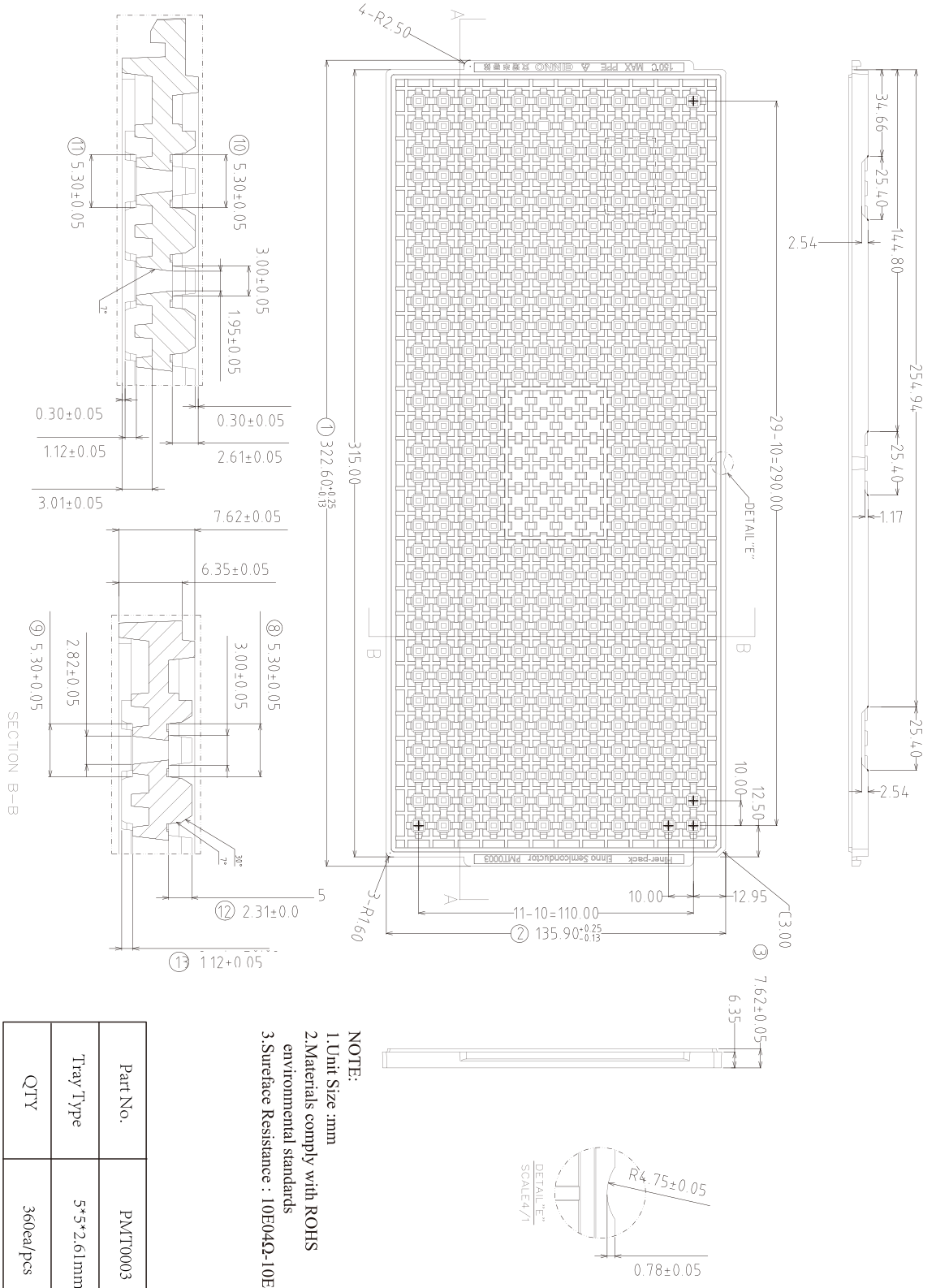


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.31	2.46	2.61
A1		2.0 BASIC	
D	4.90	5.00	5.10
D1		3.50 BASIC	
E	4.90	5.00	5.10
E1		3.50 BASIC	
e		0.50 BASIC	
c	0.42	0.46	0.50
α	0.20	0.25	0.30
b	0.30	0.35	0.40
d	0.25	0.30	0.35
f	3.95	4.00	4.05
r		0.26 BASIC	
L3		1.230 REF	
L1		0.625 REF	
L2		0.050 REF	
aaa		0.15	
ccc		0.08	

LQFN Package
34-LEAD 5.00mm x 5.00mm x 2.46mm
POD-0008-A0

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





NOTE:
1.Unit Size :mm
2.Materials comply with ROHS environmental standards
3.Sureface Resistance : 10E04Ω-10E11Ω

Part No.	Tray Type	QTY
PMT0003	5*5*2.61mm	360ea/pcs