1A Ultra-Low Noise High-PSRR High-Accuracy LDO Voltage Regulator

Features

- Input Voltage Range: 2.6V to 6.5V
- Output Voltage Range: 0.8V to 6V
- Low Quiescent Current: 210uA (TYP)
- Ultra-Low Output Noise: 6μV_{RMS}(TYP) Independent of Output Voltages
- High PSRR: Over 70dB at 1kHz and 40dB at 1MHz
- 1.0% Accuracy Over Line, Load and Temperature
- Very Low Dropout: 160mV (TYP) at 1A Load
- Fast Transient Response
- Open-Drain Power-Good (PG) Output
- Thermal Shutdown and Over-Current Protection
- Stable with a 22μF or larger ceramic capacitor
- Operating Junction Temperature: -40°C to +125°C
- 2.5mm x 2.5mm 10-Pin WSON Package

Description

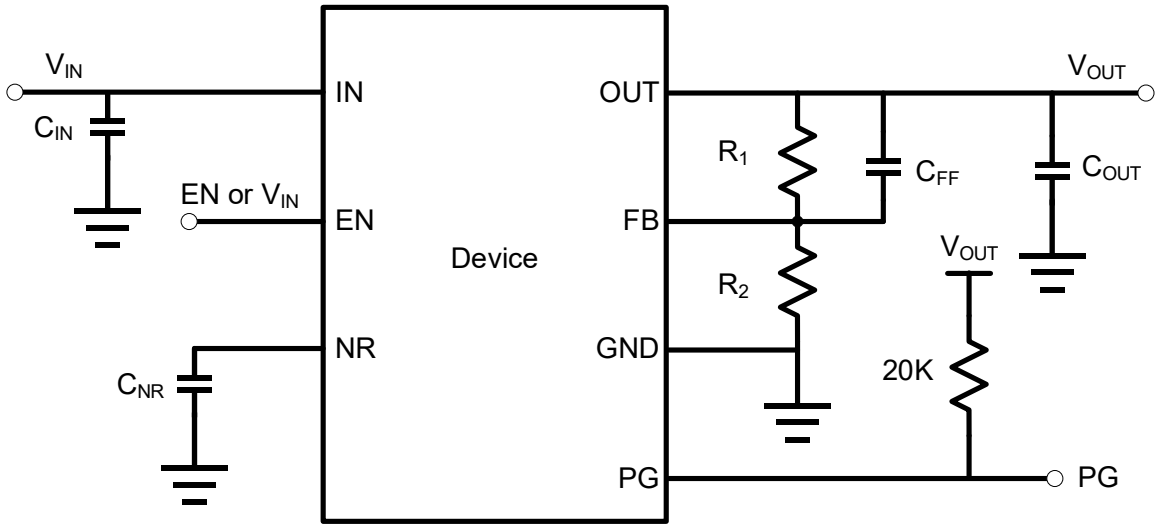
The device is an ultra-low-noise (6μV_{RMS}), high PSRR, low-dropout voltage regulator capable of sourcing 1A current. The output is adjustable with external resistors from 0.8V to 6V. The device has a wide input voltage range from 2.6V to 6.5V

The device is designed to power noise-sensitive components such as found in high-speed communications, video, medical, or test and measurement applications. The very low output noise and wideband PSRR minimizes phase noise and clock jitter for devices ranging from VCOs, ADCs, DACs, to high-end processors and FPGAs.

Applications

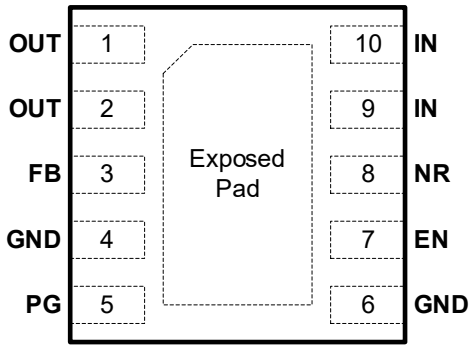
- High Performance Analog: VCO, ADC, DAC, LVDS
- Communication: CPU, ASIC, FPGA, CPLD, DSP
- Noise Sensitive Imaging: CMOC Sensors, Video ASICs
- Instrumentation, Medical, and Audio

Typical Application Circuit



Pin Configuration and Functions

2.5mm x 2.5mm 10-Pin WSON
Top View



Pin Descriptions

PIN Number	PIN Name	I/O	Function
1, 2	OUT	O	Regulator output voltage pin. A 22µF or larger ceramic capacitor from OUT to ground is required to ensure regulator stability.
3	FB	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10nF feed-forward capacitor from FB to OUT is recommended to maximize the regulator ac performance.
4	GND	-	Device ground pin.
5	PG	O	Open-drain power-good indicator pin for the LDO output voltage. A 10kΩ to 100kΩ external pullup resistor is required. This pin can be left floating or connected to GND if not used.
6	GND	-	Device ground pin.
7	EN	I	Enable pin. Drive EN high to turn on the LDO and drive the EN low to turn off the LDO. The EN pin can be connected to IN for automatic startup
8	NR	O	Noise reduction pin. A 100nF or larger capacitor from NR to GND is recommended to maximize the performance
9, 10	IN	I	Input voltage pin. A 10µF capacitor from IN to GND is recommended
-	Exposed Pad	-	Exposed Pad must be connected to a large-area ground plane to get maximum electrical and thermal performance.

Package/Ordering Information

DEVICE	PACKAGE TYPE	MARKING	PACKING OPTION
TPS7A9101DSKR	2.5mm x 2.5mm 10-Pin WSON	19GP	Tape and Reel, 3000

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
IN, PG and EN Pins	IN, PG, EN	−0.3 to 7	V
OUT Pin	OUT	-0.3 to V_{IN} + 0.3	V
NR and FB Pins	NR, FB	-0.3 to V_{IN} + 0.3	V
Storage temperature range	T_{STG}	−65 to +150	°C
Output current	I_{OUT}	Internally Limited	A

Notes:

1. Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

ESD Ratings

			Value	Unit
V_{ESD}	Electrostatic Discharge	HBM (Human Body Model)	3000	V
		CDM (Charge Device Model)	1000	

Recommended Operation Conditions

Over operating temperature range unless otherwise noted

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	2.6	6.5	V
Output Voltage	V_{OUT}	0.8	6.0	V
Output Capacitance	C_{OUT}	22		μF
Output Current	I_{OUT}	0	1	A
Operating Junction Temperature	T_J	-40	125	°C

Thermal Information

Package	$R_{\theta JA}$	$R_{\theta JC}$	Unit
WSON-10-EP(2.5x2.5)	55	21	°C/W

Electrical Characteristics

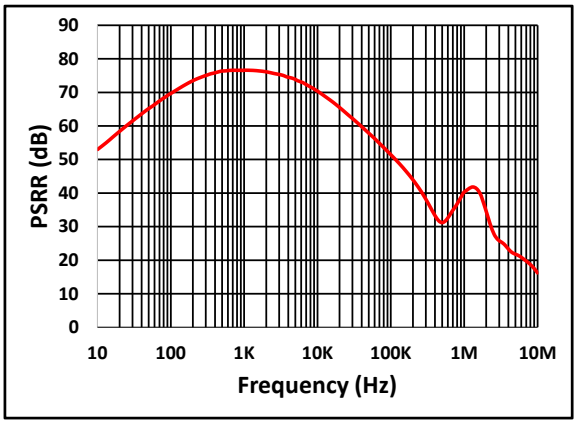
V_{IN} = 2.6V or V_{IN} = V_{OUT} + 0.5V (whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10µF, C_{OUT} = 22µF, C_{NR} = 1µF, C_{FF} = open, T_A = −40 to +125°C unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		2.6	-	6.5	V
Reference Voltage	V_{REF}			0.8		V
UVLO Threshold	V_{UVLO}	V_{IN} rising			2.5	V
UVLO Hysteresis	ΔV_{UVLO}			210		mV
Output Voltage Accuracy		5mA ≤ I_{OUT} ≤ 1A	-1.0	0	1.0	%
GND Pin Current	I_{GND}	V_{IN} = 6.5V, I_{OUT} = 1mA		210		µA
Shutdown Current	I_{SHDN}			0.2		µA
Dropout Voltage	V_{DO}	V_{IN} ≥ 2.6V, 0.8V ≤ V_{OUT} ≤ 6.0, I_{OUT} = 1A, V_{FB} = 0.8 – 3%		160		mV
Over Current Limit	I_{LIM}	V_{IN} = 2.6 – 6.5V	1			A
Line Regulation	$\Delta V_{OUT(LINE)}$	V_{IN} = 2.6 – 6.5V		0.03		%/V
Load Regulation	ΔV_{OUT} /($V_{OUT}\Delta I_{OUT}$)	I_{OUT} = 5mA to 1A		0.05		%/A
EN pin low-level input voltage (device disabled)	$V_{IL(EN)}$		0		0.4	V
EN pin high-level input voltage (device enabled)	$V_{IH(EN)}$		1.35		6.5	V
EN PIN Leakage Current	I_{EN}	V_{IN} = 6.5V, 0V ≤ V_{EN} ≤ 6.5V	-0.2		0.2	µA
FB PIN Leakage Current	I_{FB}	V_{IN} = 6.5V, V_{FB} = 0.8V	-0.2		0.2	µA
PG Pin Threshold	V_{PG}	V_{OUT} Falling, PG Transitioning Low Expressed as a Percentage of $V_{OUT(TARGET)}$		88%		
PG Pin Hysteresis	$V_{hys(PG)}$	V_{OUT} Rising, PG Transitioning High Expressed as a Percentage of $V_{OUT(TARGET)}$		2%		
PG Pin Low Level Output Voltage	$V_{OL(PG)}$	V_{OUT} < V_{PG}, Source 1mA to PG Pin			0.4	V
PG Pin Leakage Current	I_{PG}	V_{OUT} > V_{PG}, Apply 6.5V to PG Pin			1	µA

Power Supply Rejection Ratio	PSRR	V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{OUT} = 22µF, C_{NR} = 1µF, C_{FF} = 10nF	f = 1kHz		75		dB
			f = 100kHz		52		
			f = 1MHz		41		
Output Noise Voltage	V_N	BW = 100Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{OUT} = 22µF, C_{NR} = 1µF, C_{FF} = 100nF			6.0		μV_{RMS}
Thermal Shutdown Temperature	TSD				160		°C
Thermal Shutdown Hysteresis	T_{HYS}				20		°C

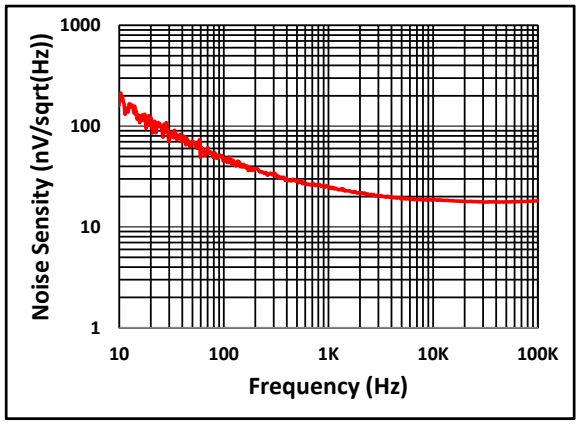
Typical Characteristics

V_{IN} = 2.6V or V_{IN} = V_{OUT} + 0.4V (whichever is greater), OUT connected to 50Ω to GND, V_{EN} = V_{IN}, C_{IN} = 10µF, C_{OUT} = 22µF, C_{NR} = 1µF, C_{FF} = open, T_A = −40 to +125°C unless otherwise noted



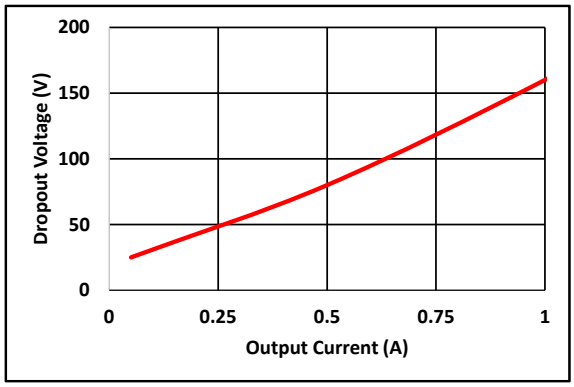
V_{IN} = 4V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{OUT} = 22µF, C_{NR} = 1µF, C_{FF} = open

Fig. 1 PSRR



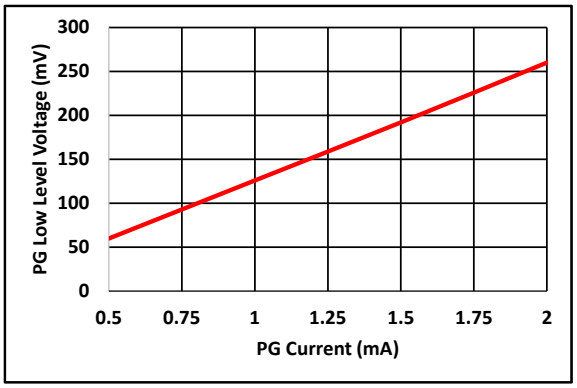
V_{IN} = 4V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{OUT} = 22µF, C_{NR} = 1µF, C_{FF} = open

Fig. 2 Output Noise Density



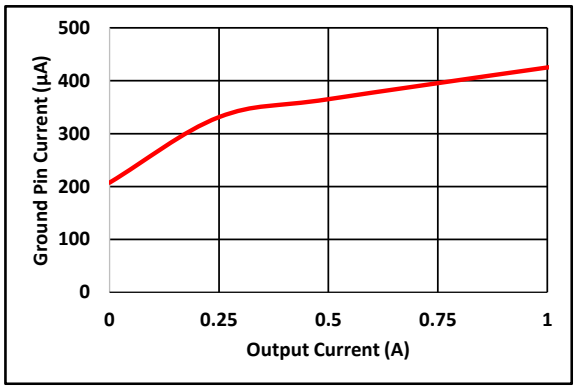
V_{IN} = 3.3V, V_{EN} = 3.3V

Fig. 3 Dropout Voltage



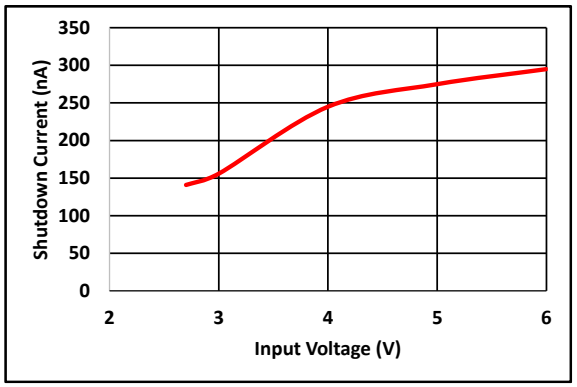
V_{IN} = 6V

Fig. 4 PG Low Level Voltage vs Current



V_{IN} = 4V, V_{OUT} = 3.3V, C_{OUT} = 22µF

Fig. 5 Ground Current vs Output Current



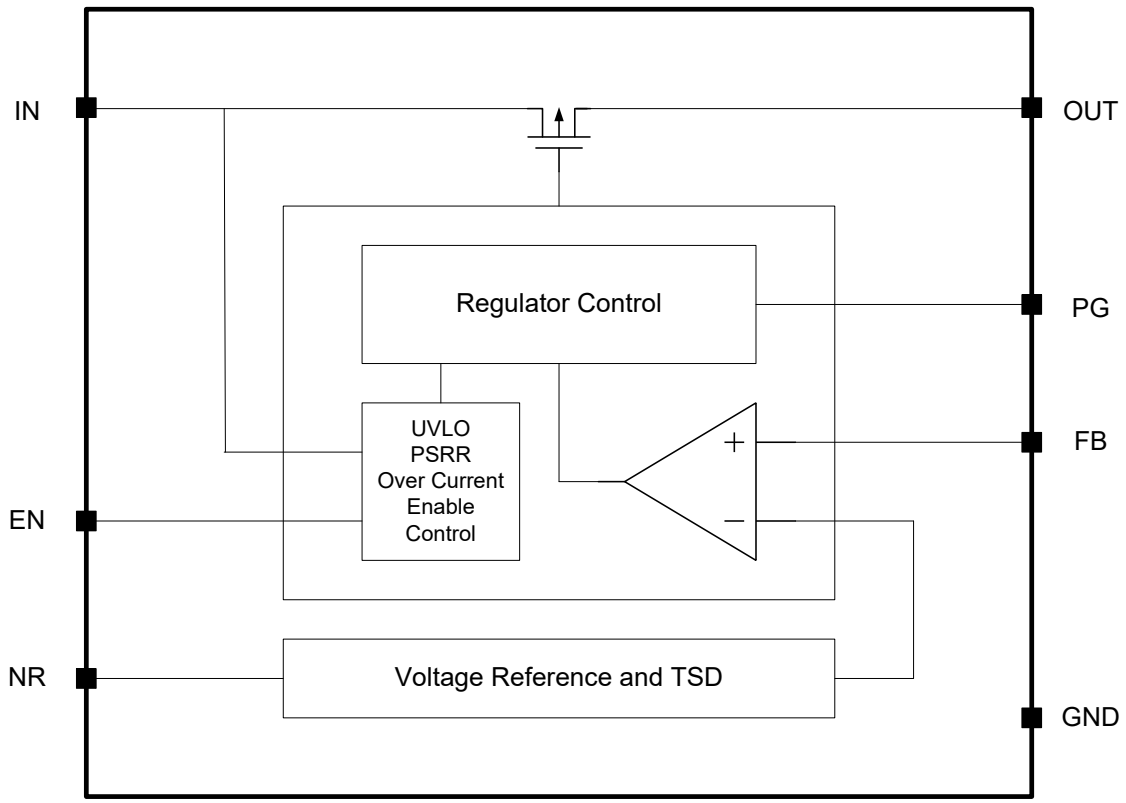
V_{EN} = 0V

Fig. 6 Power Down Current vs Input Voltage

Functional Description

The device is a low-noise, high PSRR low dropout (LDO) regulator capable of sourcing a 1A load current with 160mV dropout voltage. The device can operate down to 2.6V input voltage and a 0.8V output voltage. This combination of low-noise, high PSRR, and low dropout voltage makes the device an ideal LDO to power a multitude of load from noise-sensitive communication components in high-speed communications applications to high-end microprocessors or field-programmable gate arrays (FPGAs). The device also features internal protection circuity (such as the under-voltage lockout) which prevents the device from turning on before the input is high enough to ensure accurate regulation. Foldback current limiting is also included, allowing the output to source the rated output current when the output voltage is in regulation but reduces the allowable output current during short-circuit conditions. The internal power-good detection circuit allows users to sequence down-stream supplies and be alerted if the output voltage is below a regulation threshold.

Functional Block Diagram



Feature Description

Enable

The enable pin for the device is active high. The device is enabled when the enable pin voltage is greater than $V_{IH(EN)}$ and disabled with the enable pin voltage less than $V_{IL(EN)}$. If independent control of chip enable is not needed, then connect the enable pin to the input. The device has an internal pulldown MOSFET that connects a discharge resistor from VOUT to ground when the device is disabled to actively discharge the output voltage.

Dropout voltage

Dropout voltage (V_{DO}) is defined as the VIN – VOUT voltage at the rated current of 1A, where the pass transistor is fully on and in the linear region of operation. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain in regulation. If the input falls below the nominal output regulation, then the output follows the input.

Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. The device features an output voltage accuracy of 2% that includes the errors introduced by the internal reference, load regulation, and line regulation variance across the full range of rated load and the line operating conditions over temperature.

Undervoltage Lockout (UVLO)

The device uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage, the PG pin open-drain output engages and pulls the PG pin close to ground. When the feedback voltage exceeds the threshold by an amount greater than $V_{HYS(PG)}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, and downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Using a pullup resistor from 10kΩ to 100kΩ is recommended.

Internal Current Limit

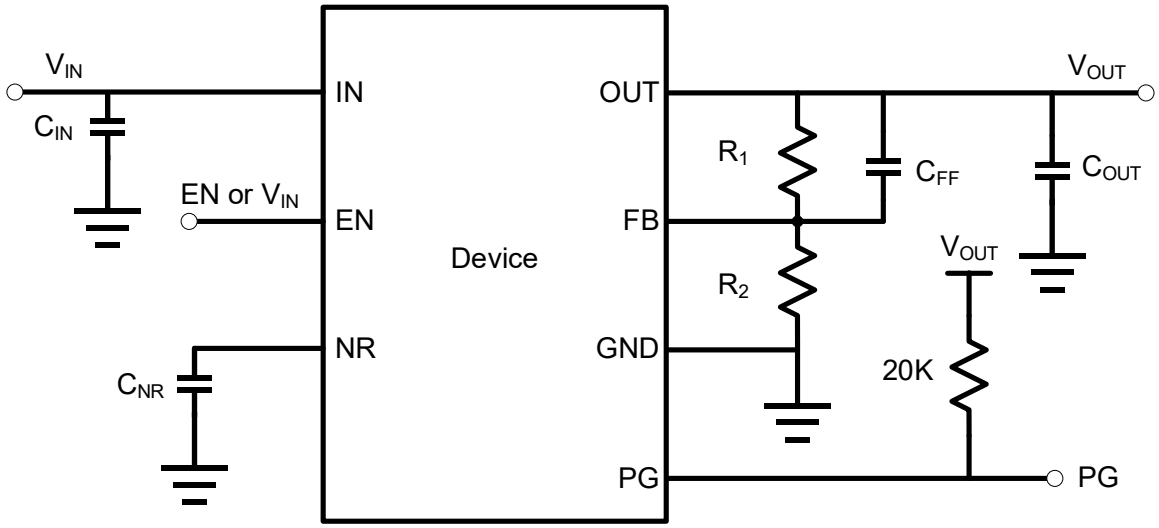
The internal current-limit circuit is used to protect the LDO against transient high-load faults or shorting events. The LDO is not designed to operate in current limit under steady-state conditions.

Thermal Protection

The device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO.

Application Information

Typical Application



The diagram above shows a typical application circuit.

Input Capacitor and Output Capacitor

The device is designed and characterized for operation with ceramic capacitors of 10μF or greater at the input and 22μF or greater at the output. Locate the input and output capacitors as near as practical to the input and output pins to minimize the trace inductance from the capacitor to the device.

Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}), from the FB pin to the OUT pin is not required to achieve stability, a 10nF, feed-forward capacitor improves noise and PSRR performance.

Adjustable Output

The output voltage of the device can be adjusted from 0.8V to 6V by using a resistor network as shown in the typical application diagram.

The table below lists the resistor combination required to achieve a few of the most common rails using commercially available, 0.1%-tolerance resistors.

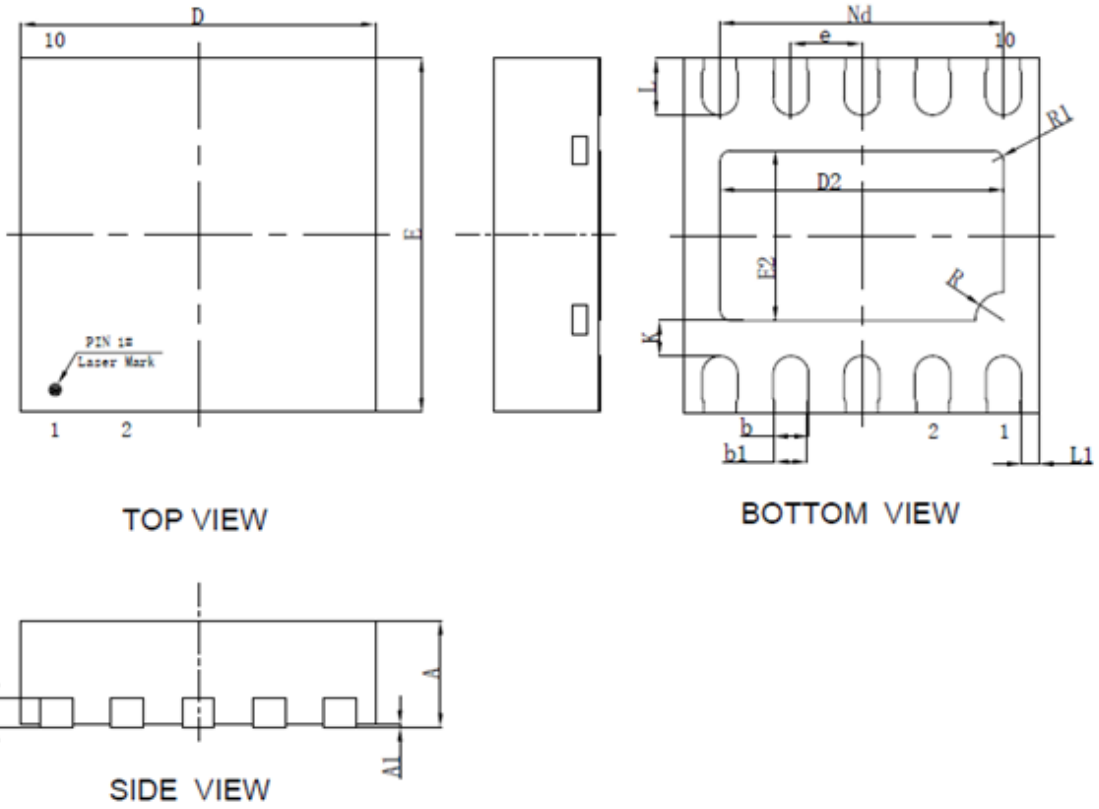
VOUT(TARGET) (V)	FEEDBACK RESISTOR VALUES		CALCULATED OUTPUT VOLTAGE (V)
	R1 (kΩ)	R2 (kΩ)	
0.8	Short	Open	0.800
1.00	2.55	10.2	1.000
1.20	5.9	11,8	1,200
1.50	9.31	10.7	1.496
1.80	1.87	1.5	1.797
2.50	2.43	1.15	2.490
3.00	3.16	1.15	2.998
3.30	3.57	1.15	3.283
5.00	10.5	2	5.00

Layout Guidelines

General guidelines are to place all circuit components on the same side of the circuit board and as close as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections would negatively affect system performance.

PACKAGE OUTLINE DIMENSIONS

2.5mm x 2.5mm 10-PIN WSON Package



Symbol	Dimensions (mm)			Symbol	Dimensions (mm)		
	Min	Typ	Max		Min	Typ	Max
A	0.70	0.75	0.80	Nd	2.00BSC		
A1	0	0.02	0.05	E	2.40	2.50	2.60
b	0.20	0.25	0.30	E2	1.10	1.20	1.30
b1	0.23REF			L	0.35	0.40	0.45
c	0.203REF			L1	0.125REF		
D	2.40	2.50	2.60	R	0.20REF		
D2				R1	0.075REF		
e	0.50BSC			K	0.25REF		