WS2994 Fast turn-off Dual LLC Synchronous Rectifier Controller

Description

WS2994 is a high performance dual channel synchronous rectifier controller, which is applied to the output side rectifier of half bridge LLC resonant converter, and can realize the optimal control of MOSFET. By detecting the Vds voltage of the rectified MOSFET, the MOSFET can be reliably switched on and off, thereby replacing Schottky diodes and improving the efficiency of the half-bridge LLC converter.

WS2994 Gate voltage can be regulated according to output load with different turn-on delay time,avoiding false turn-on because of capacitive current during light load.

The WS2994 is Green, when the load current reduce to a certain level, the gate drive is turned off, thus limiting the IC current to less than 140uA. The fast shutdown capability of the WS2994 supports continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operation.

It is highly-integrated with SOP8 package.

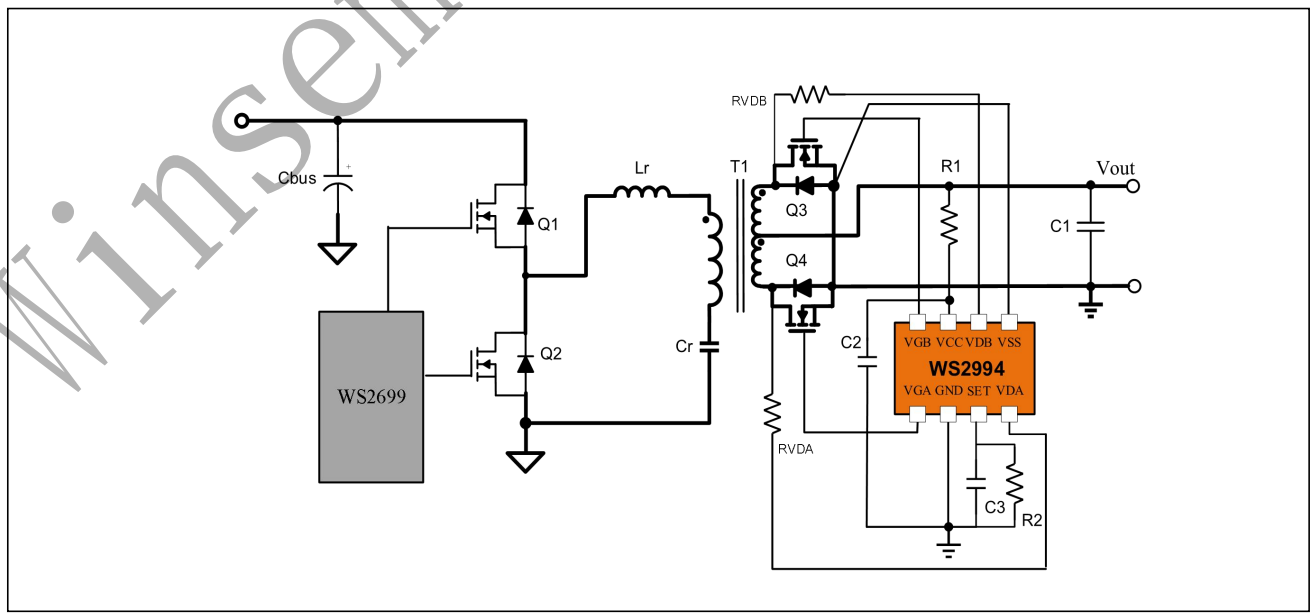
Features

- VDA, VDB can withstand 120V
- Wide VCC Operation Range,Support 4.83V ~ 35V
- 140uA Low Quiescent Current in Light Load Mode
- Fast Turn-Off ,Support CCM/CrCM/DCM
- High level up to 11.5V for Driver
- Interlock function for Channel A&B
- SOP8 Package

Typical Application

- AC/DC Adapters
- PC Power Supply
- LCD TV Power Supply
- Industry and Medical Power Supply

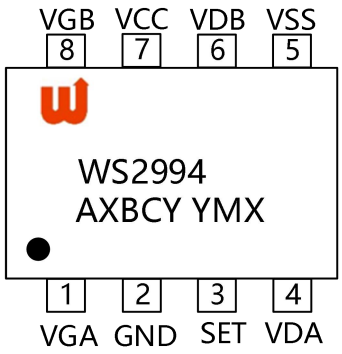
Typical Application Circuit



Note: VDA\VDB must be connected with resistance, recommended value: 200Ω -- 2.0kΩ, two resistance values can be different.

Pin Configuration and Marking Information

WS2994 is available in SOP8 package.The top marking is shown as below:



WS2994：Product Code
A：Product Code
X：Internal Code
BCY：Internal QC Code
YMX：D/C

Ordering Information

Package	Marking	Part Number
8-Pin SOP8,Pb-free	WS2994	WS2994

Absolute Maximum Ratings(1)

Parameter	Limit	Unit
VCC to VSS	-0.3~38	V
GND to VSS	-0.3~0.3	V
VGA,VGB to GND	-0.3~20	V
VDA,VDB to to VSS	-0.8~120	V
SET to VSS	-0.3~6.5	V
Power Dissipation(2)（Ta=25℃）	1.4	W
Operation Junction Temperature	150	℃
Lead Temperature（10s）	260	℃
Storage Temperature	-55~150	℃
θ_{JA}	90	℃/W
θ_{JC}	45	℃/W

Note 1: Stresses above those listed Absolute Maximum Ratings may cause permanent damage to the device.

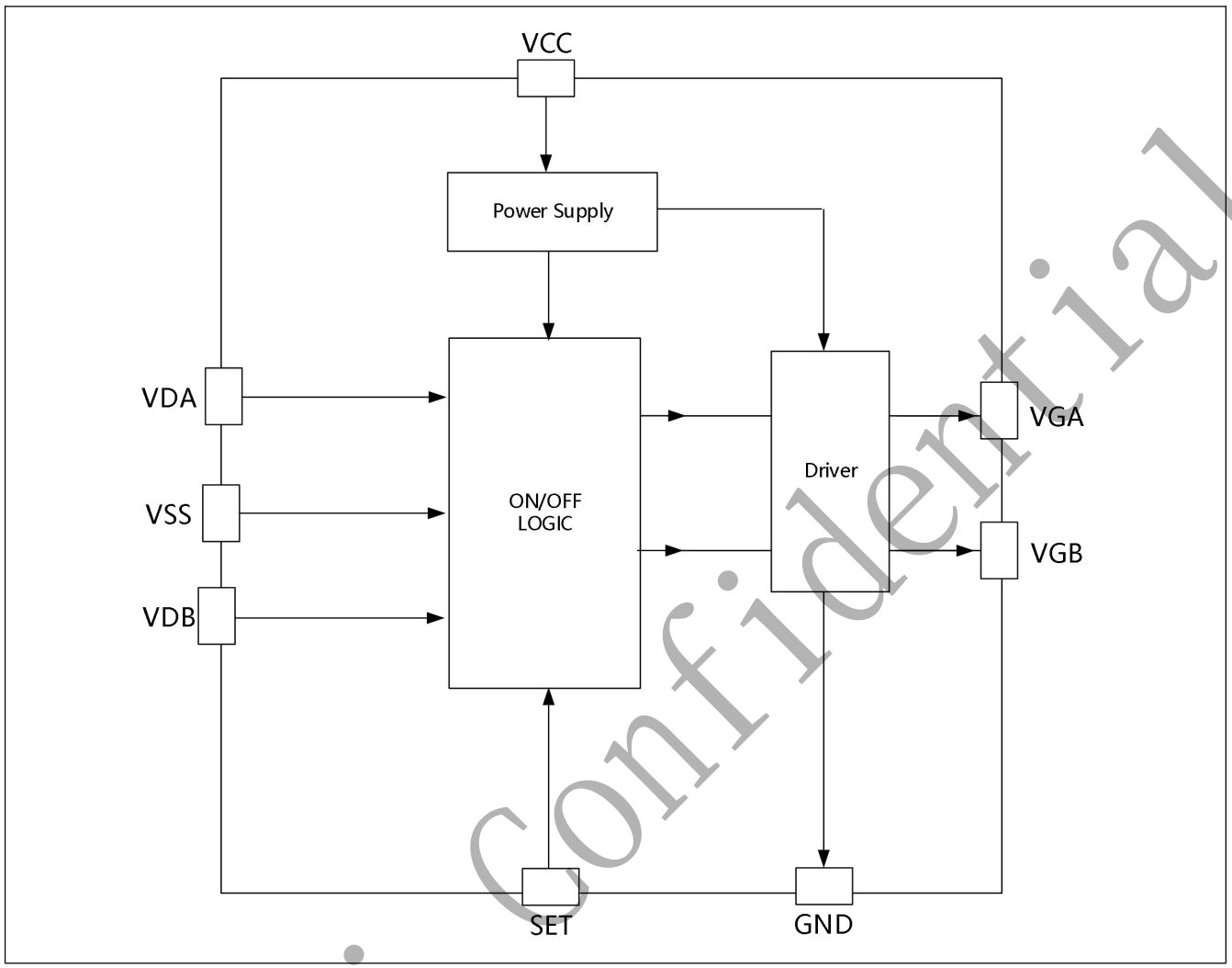
Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J(MAX)}$, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Recommended Operation Conditions(3)

Symbol	Value	Unit
VCC to VSS	5~35	V
T_j	-40~125	℃

Note 3:The device is not guaranteed to function outside of its operating conditions.

Block Diagram



Pin Definition

Pin No.	Pin Name	Function Description
1	VGA	Gate Driver Output for Channel A.
2	GND	IC Power Ground.
3	SET	V_{th_off2} set pins，If the voltage is less than 0.35V, enter the Disable mode
4	VDA	Drain Sense Input for Channel A.
5	VSS	Used as reference for VDA and VDB voltage sampling
6	VDB	Drain Sense Input for Channel B.
7	VCC	IC Power Supply，VCC up to 35V.
8	VGB	Gate Driver Output for Channel B.

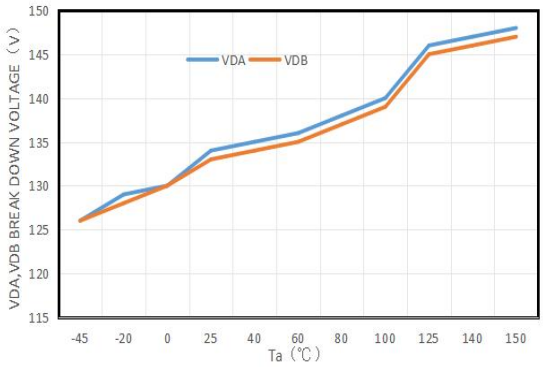
Electrical Characteristics

Condition：VCC=12V，T_J=25℃. (unless otherwise noted)

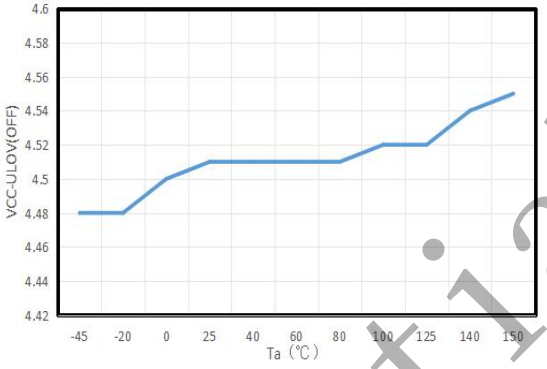
Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage(VCC)						
VCC voltage range	$V_{CC-Range}$		4.83		35	V
UVLO(OFF)	V_{CC-on}		4.37	4.6	4.83	V
UVLO Hysteresis	V_{CC-hys}		0.31	0.35	0.39	V
VCC Operating current	I_{CC}	CLOAD = 4.7nF, FSW = 100kHz	12	15.5	19	mA
VCC Quiescent operation current	I_Q	IC Enable without Gate Driver	1.8	2.3	2.8	mA
Light Load Mode Current	I_{GM}	Under Light Load Mode	110	150	190	uA
Control Circuitry(VDA,VDB, VSS)						
Turn on threshold	V_{th_on}	V_{CC}=12V	-320	-260	-200	mV
Vds Regulation threshold	$V_{th-off2}$		-26	-20	-14	mV
Turn off threshold	V_{th-off}		41	48	55	mV
Turn-on Delay@Heavy Load	T_{don}	T_{GM}<T_{GM_EXIT}	72	100	130	ns
Turn-on blanking time	T_{bon}	C_{LOAD}=4.7nF	0.4	0.8	1.2	us
Turn-off blanking time	T_{boff}	C_{LOAD}=4.7nF	1.2	1.6	2	us
Inter lock time	$T_{interlock}$	Guaranteed by design		200		nS
Light Load Control						
Turn off threshold	V_{th-b}	Enable after T_{bon}	1.6	2	2.4	V
Entry Time for Light-Load	T_{GM-ENT}		34.5	45	56.5	us
Exit Time for Light-Load	$T_{GM-EXIT}$			1		Cycle
IC Enable（SET）						
IC Disable	V_{IC-DIS}		0.26	0.35	0.45	V
Gate Driver(GATE)						
V_G (high)		Vcc=12V~35V	10	11.5	13	V
V_G (low)		VG sink 100mA	0.035	0.06	0.085	V
Maximum source current	I_{SOURCE}	Guaranteed by design		200		mA
Pull-down impedance	I_{Sink}	VG sink 100mA	0.35	0.6	0.85	Ω
Turn-off total delay	$T_{D-Gateoff}$	V_{DA}=V_{SA}, C_{LOAD}=1nF, R_{GATE}=0Ω, V_{GS}=2V	20	30	40	ns
		V_{DA}=VSA, C_{LOAD}=4.7nF, R_{GATE}=0Ω, V_{GS}=2V	30	45	60	
In-Chip OTP						
OTP Enter	T_{OTP}	Guaranteed by design	145	160	175	℃
OTP Exit	$T_{OTP-hys}$	Guaranteed by design	10	20	30	℃

Typical Performance Characteristics

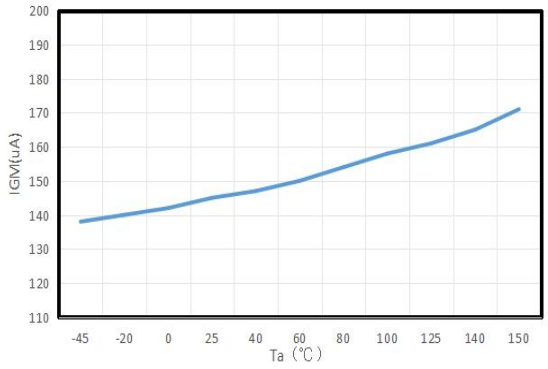
VDA,VDB Breakdown Voltage vs. Temperature



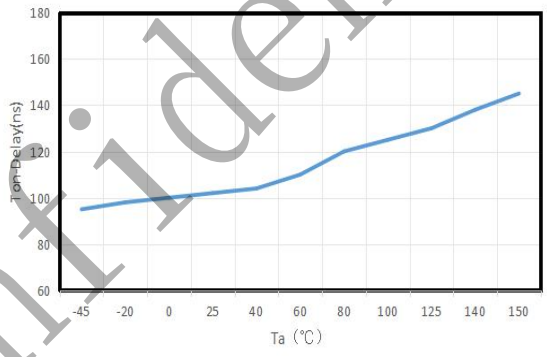
VCC UVLO(OFF) vs. Temperature



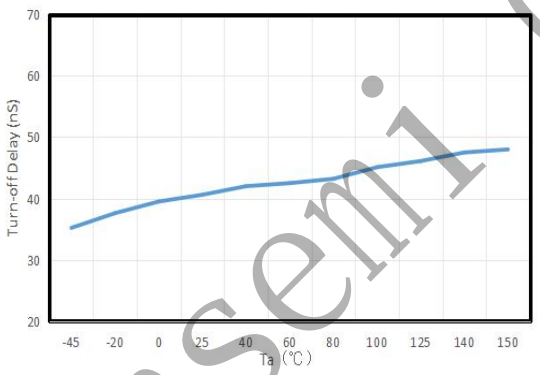
Light Load Mode Current vs. Temperature（VCC=24V）



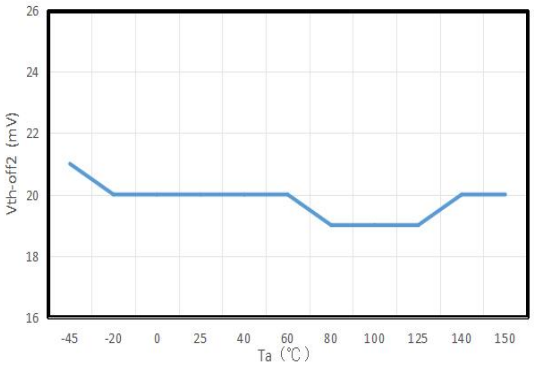
Turn-On Delay vs. Temperature(CLOAD = 1nF)



Turn-Off Delay vs. Temperature(CLOAD = 4.7nF)



Vds Regulation threshold (VSS - VD) vs. Temperature



Function Description

The WS2994 is a dual-channel controller for rectifier on the output side of the half-bridge LLC resonant converter, which supports CCM, CrCM and DCM and automatically realizes optimal control. The WS2994 has simple periphery and reliable protection. The following chapters introduce its various functional modules in detail.

Start-Up and Under-Voltage Lockout (UVLO)

The WS2994 VCC withstand up to 35V.When VCC voltage is under UVLO threshold,WS2994 enter in sleep mode and keep the VGA&VGB low. When VCC rises above UVLO threshold, IC starts operating.

Enable(SET)

If the SET pin voltage is less than 0.35V, WS2994 will turn off the driver output, and the IC working current is less than 140 uA. When the SET signal is pulled up again, the drive signal can only resume work when the next rectification cycle arrives.

Programmableregulation threshold（SET）

With the SET pin resistance, the value of V_{th_off2} can be fine-tuned. When Rset ≥100KΩ, V_{th_off2} is -20mV. When Rset <100KΩ, the value of V_{th_off2} decreases linearly and can be adjusted to a maximum of 12mV. The SET pin needs to connect a ceramic capacitor to GND to filter the noise; The larger the capacitance of the SET pin, the better the filtering effect, but the starting time will be longer, and these both sides need to be taken into account; General recommended value: 10nf.

It is recommended that the SET pin resistor value not be less than 33KΩ. If the resistance value is less than 33KΩ,WS2994 has the risk of turn off the driver output, the chip will enter the energy saving mode.

The following chart shows the Vth-off2 thresholds for different resistance values:

Rset（KΩ）	NC	100.0	91.0	82.0	75.0	68.0	56.0	47.0	33.0
Vth-off2(-mv)	20.0	21.0	23.0	25.0	26.0	27.0	29.0	30.0	32.0

First on-cycle blanking

After the IC is enabled, or when exiting the energy saving mode, in order to prevent the SR from being turned on during the body diode on and prevent the pass-through phenomenon caused by MOSFET, the IC will shield the first on-tube cycle, and the next on-off cycle will begin to enter the normal MOSFET on-off control.

MOSFET ON/OFF control

Vds drops blew V_{th_on} when current pass through parasitic body diode of MOSFET, IC will output driver signal after T_{don} delay, which is shown in Figure 1.

When the MOSSFET is turned on, the Tbon will be maintained for a period of time, called the turn on shielding time (about 0.9us), to prevent false shutdown caused by ringing.

When the MOSFET Is turned on, the voltage Vds at both ends of the MOSFET follows the secondary current Is. As the current flowing through the switch decreases, when the Vds forward voltage drop exceeds V_{th_off2} (be programmed from -20mV to -32mV), a larger internal pull-down current source takes effect, and the driving voltage decreases with a larger slope. As the Vds forward voltage drop continues to rise to the shutdown threshold V_{th_off}, the internal pull-down takes effect and the Gate drive voltage is pulled to 0V after a very short shutdown delay. During the Tbon time, the value of V_{th_off} will be adjusted to +90mV to ensure that the Gate driver can still be turned off during the Tbon

time to ensure safety in some extreme cases.

In CCM mode, this feature keeps the gate voltage at a very low level when the SR MOSFET is turned off, increasing the turn-off speed.

When the Gate of driver is turned Off, the blanking time starting to be counted, the gate driver remains off for the Tboff time.

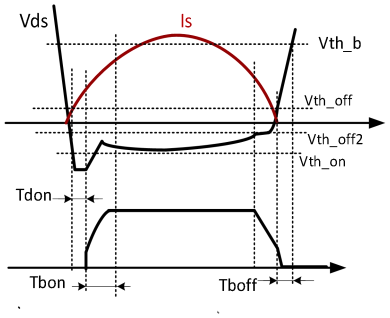


Figure 1 ON/OFF control logic

Burst-mode control

In order to avoid the pre-LLC system being in burst-mode, which would cause the secondary synchronous rectifier controller to turn on incorrectly, the WS2994 has a patented control circuit built in. When WS2994 detects that the system enters Burst-mode, it will increase the drive delay and decrease the drive current. In addition to the two mechanisms mentioned above, WS2994 also adds that the system does not send driver signals in the first cycle after exiting from burst-mode, and outputs driver signals in the next cycle.

Channel Interlock

The WS2994 incorporates an interlock function. The interlock function avoids the turn on of both gate driver outputs at the same time.

After turn-off of one gate driver output, the IC waits typically 200 ns ($T_{interlock}$) before turning on the other gate driver output.

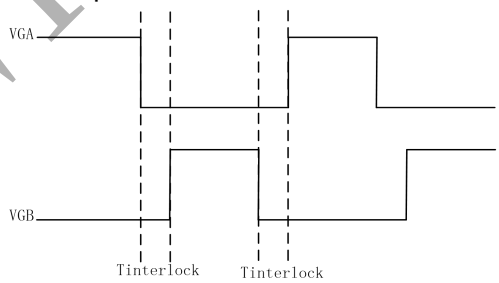


Figure 2 Interlock function

Thermal Shutdown

When the junction temperature of the IC is higher than the over-temperature protection threshold, the driver will be shutdown and enters in OTP mode. And IC will exit OTP mode when the junction temperature decrease 20 degree .

PCB Layout Guidelines ：

1，VDA and VDB respectively form two detection loops with VSS,VDA/VSS, VDB/VSS as close as possible to each MOSFET (drain/source), the loop is as small as possible; The two detection loops are separated as far as possible and drawn as two independent small loops.

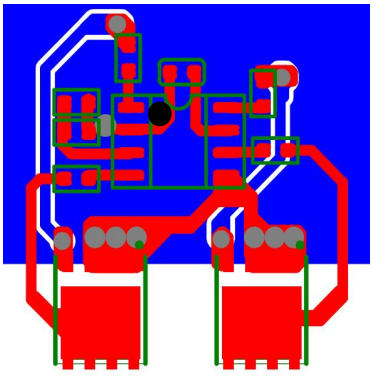
2，Place a decoupling capacitor no smaller than 1μF from VDD to PGND close to the IC for adequate filtering.

3，SET pin needs to add a capacitor to filter out interference; Capacitance and resistance as close to the pin as possible.

4，It is highly recommended to place the driver's sensing loop trace away from the power loop trace. The sensing loop trace and power loop trace can be placed on different layers to keep them separate from each other.Do not place the driver IC inside the power loop; this may affect MOSFET voltage sensing.

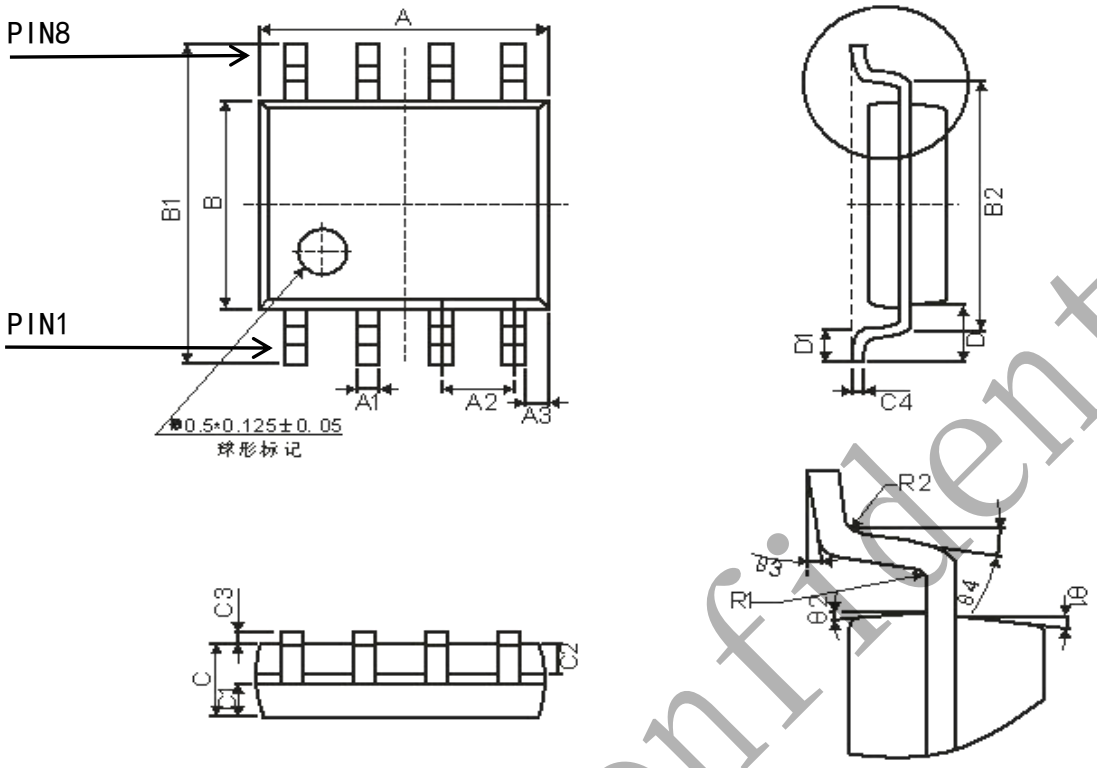
5，The VSS pin must be connected to the SR MOSFET source pin as much as possible. It minimizes errors caused by voltage difference on PCB tracks because of parasitic inductance in combination with large dI/dt values.

Layout Example：



Bottom Layer Top Layer Via PIN1

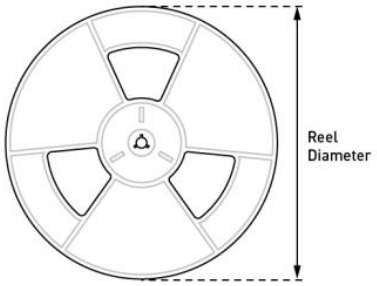
SOP8 Package Dimension

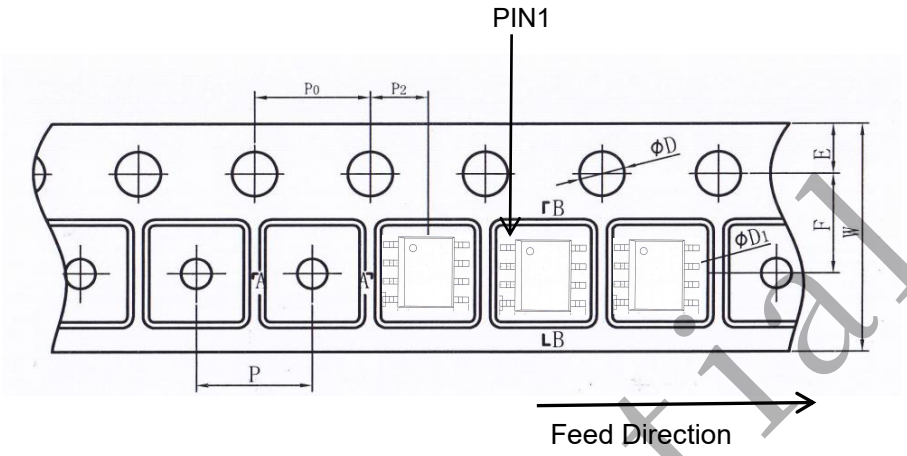


Symbol	Winsemi			
	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	4.70	5.10	0.185	0.201
B	3.70	4.10	0.146	0.161
C	1.30	1.50	0.051	0.059
A1	0.35	0.48	0.014	0.019
A2	1.27TYP		0.05TYP	
A3	0.345TYP		0.014TYP	
B1	5.80	6.20	0.228	0.244
B2	5.00TYP		0.197TYP	
C1	0.55	0.70	0.022	0.028
C2	0.55	0.70	0.022	0.028
C3	0.05	0.225	0.002	0.009
C4	0.203TYP		0.008TYP	
D	1.05TYP		0.041TYP	
D1	0.40	0.80	0.016	0.031

Shipping Packing Information:

Reel Dimensions：





Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
13in	12±0.1mm	8±0.1mm

Packing quantity specification

Part Number	Package Description	Quantity/Reel	Reel/Box	Box/Carton	Quantity/Carton
WS2994	SOP-8	4000	2	5	40000

NOTES:

1. Please recognize the company's trademark when purchasing, and contact the company headquarters if you have any questions.
2. Please do not exceed the absolute maximum rating of the device during circuit design, otherwise it will affect the reliability of the whole machine.
3. This manual is subject to version change without further notice.

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