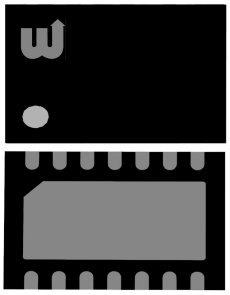
WST5010AN-L

Smart High-Side Power Switch Single Channel，9mΩ，DFN9×6-14L ，*AEC-Q100 qualified*

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 24 V and 48 V trucks + trailer and transportation systems

Package	DFN9×6-14L
Marking	WST5010ANL



Features

- PRO-SIL™ ISO 26262-ready for supporting the integrator in evaluation of hardware element according to ISO 26262:2018 Clause 8-13
- Single channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Optimized electromagnetic compatibility
- Very low electromagnetic susceptibility
- Adjustable current limitation

Diagnostic Functions

- Proportional load current sense
- High current sense precision for wide range currents
- Off-state open load detection
- OUT short to VS detection
- Overload and short to ground latch-off
- Thermal shutdown latch-off
- Very low current sense leakage

AEC Qualified

RoHS

ISO 26262 ready

Halogen-free

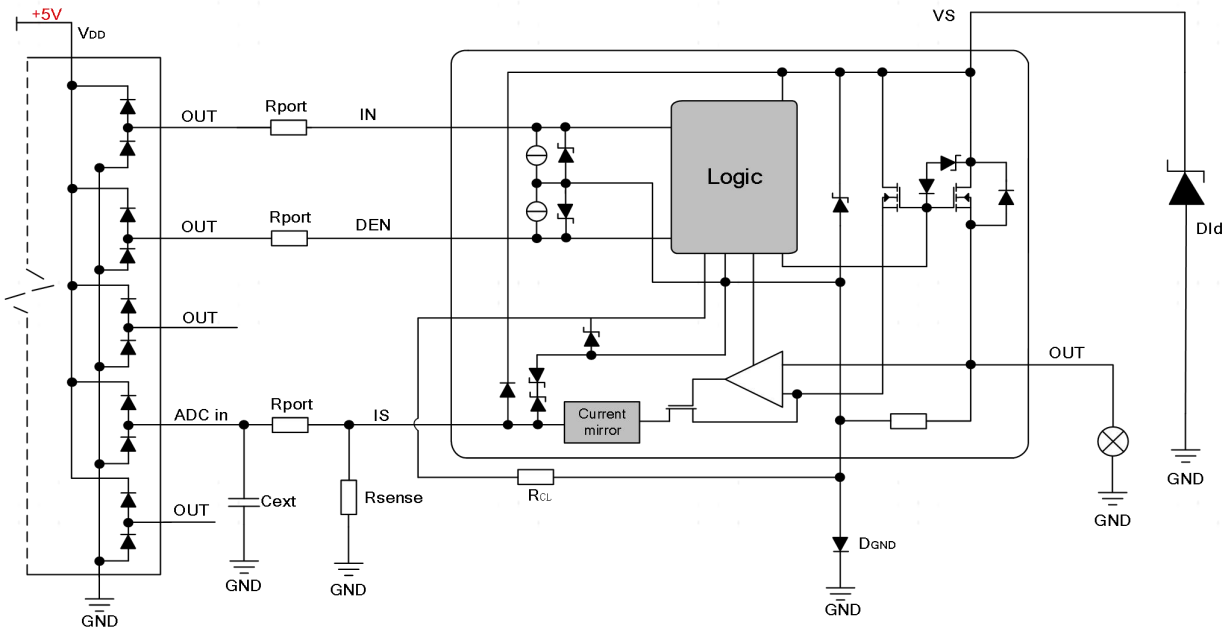
Protection Functions

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of VS
- Thermal shutdown

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage(T_j≥25 °C)	V_S	70V
Operating voltage range	V_{NOM}	5-58V
On-state resistance (T_j = 25℃)	R_{ON}	9mΩ
Nominal load current (T_j = 25℃)	$I_{L(NOM)}$	12A
Typical current sense ratio (I_{OUT}=4A)	K	5200
Current limitation	I_{LIMH}	Adjustable
Supply current in sleep	I_{SLEEP}	5uA

Typical Application Circuit

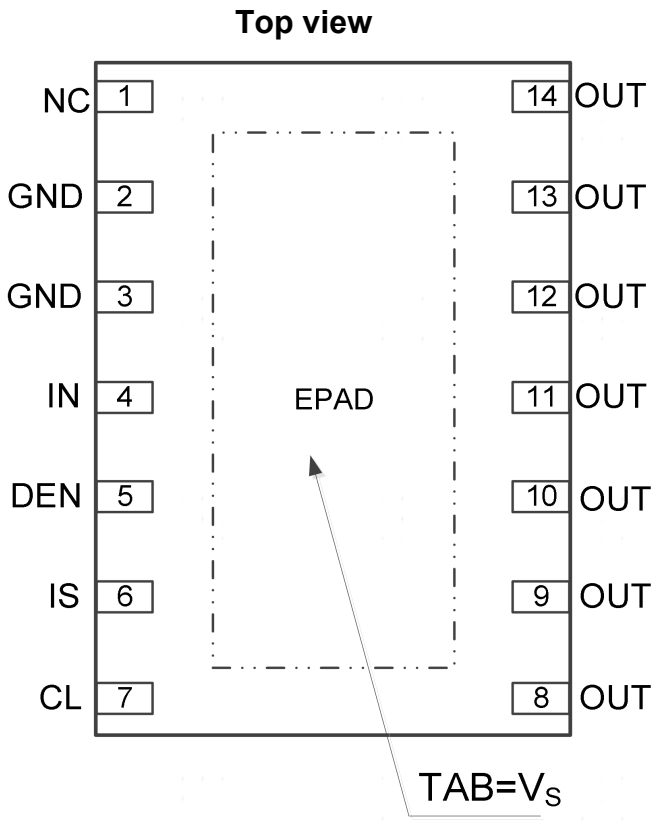


Note1：For D_{GND}, the diode with lower V_F is advisable.

Ordering Information

Package	Top Mark	Part No.
DFN9×6-14L, Pb-free	WST5010ANL XXYMXX	WST5010AN-L

Pin Configuration



Pin Description

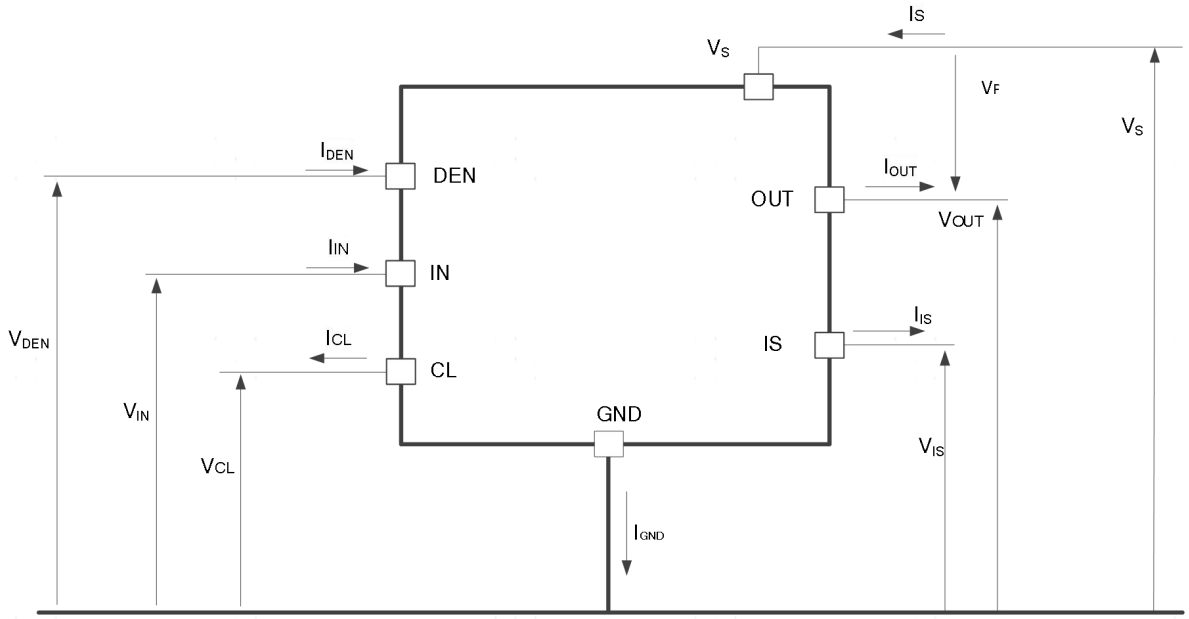
Pin Name	Pin NO.	Pin Description
NC	1	Not Connected
GND	2/3	Ground connection. Must be reverse battery protected by an external diode.
IN	4	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
DEN	5	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the IS diagnostic pin.
IS	6	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current.
CL	7	Adjustable current limit, floating if external current limit is not need.
OUT	8/9/10/11/12/13/14	Power outputs.
VS	EPAD	Battery connection.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	IS	OUT	IN	DEN
Floating	Not allowed	X(1)	X	X
To ground	Through 1.0K resistor	Not allowed	Through 15K resistor	Through 15K resistor

Note2：X do not care.

Current and Voltage Conventions



Note3: $V_F = V_{OUT} - V_S$ during reverse battery condition.

Absolute Maximum Ratings (Note4)

Symbol	Parameter	Value	Unit
V_s	Transient supply voltage	65	V
$-V_s$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	50	mA
I_{OUT}	OUT DC output current	Internally limited	A
V_{IN}, V_{DEN}	IN, DEN DC input voltage	-0.3 to 6.0	V
I_{IS}	IS pin DC output current	20	mA
	IS pin DC output current in reverse	-20	
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note4：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Thermal Resistance (Note5)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	℃/W
T_{JA}	Junction-to-Ambient Thermal Resistance	30	℃/W

Note5：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

ESD Susceptibility (Note6)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$ 3)	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_S connected (HBM)	±4	kV
$V_{ESD(CDM)}$ 4)	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	±750	V

Note6：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

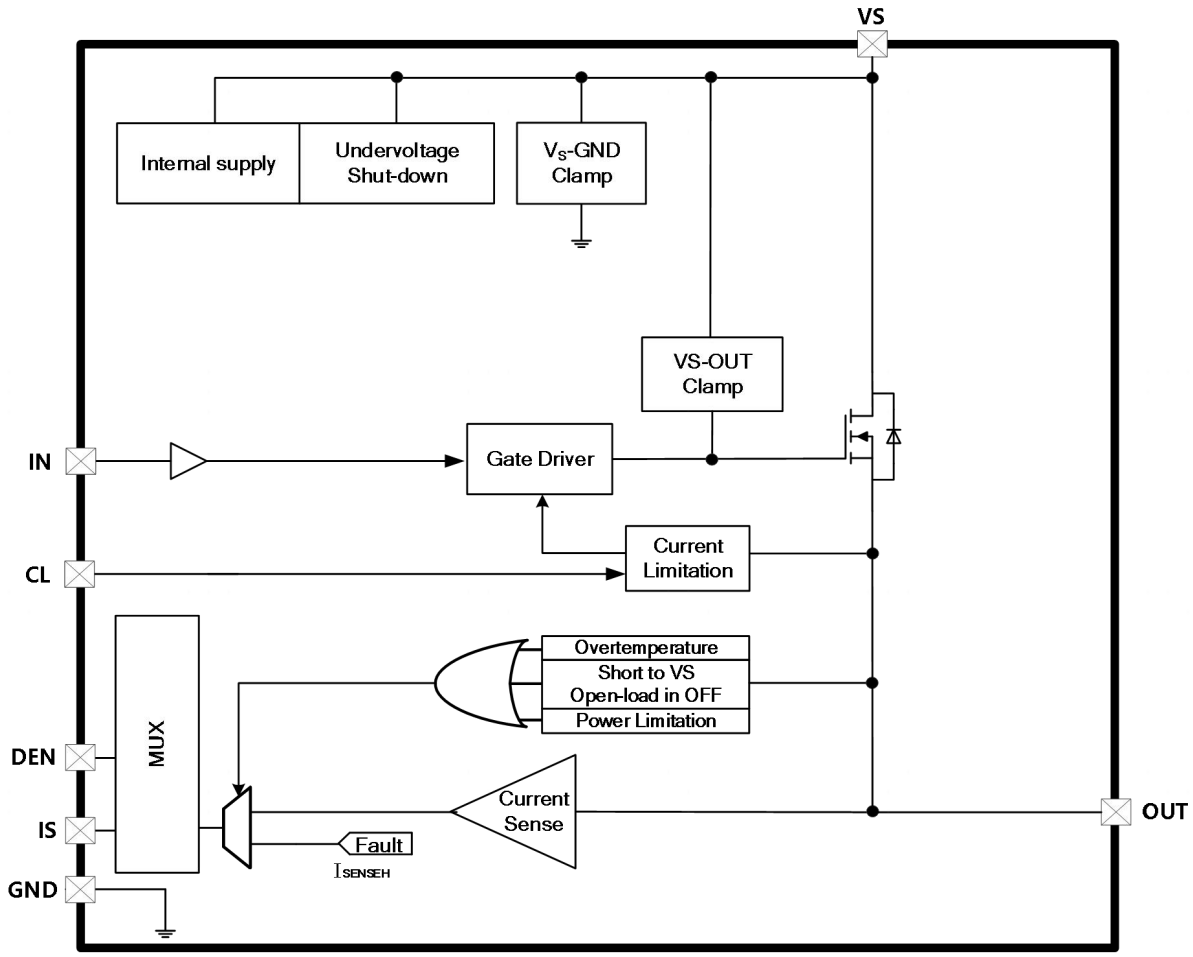
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

EAS Susceptibility (Note7)

Symbol	Parameter	Values			Unit	Note or Test Conditon
		Min.	Typ.	Max.		
E_{AS}	Maximum Energy Dissipation Single Pulse			300	mJ	I_{OUT} = 12A $T_{J(0)}$ = 150 °C V_S = 48V

Note7：Not subject to production test - specified by design.

Functional Block



Electrical Characteristics (Note8) , 5V < V_S < 58 V; -40°C < Tj < 150°C, unless otherwise specified

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Nominal operating voltage	V_{NOM}		5	48	58	V
Under voltage shutdown	V_{USD}			3.5	4.5	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_{OUT}=5A, T_j = 25℃		9		mΩ
		I_{OUT}=5A,T_j =150℃			18	
		I_{OUT}=5A,V_S =5V, T_j = 25℃			14	
Nominal load current	$I_{L(NOM)}$	T_A=25℃		13		A
Nominal load current at T_A=85℃	$I_{L(NOM)\_85}$	T_A=85℃, T_j < 150℃		10		A
Inverse Current Capability	$I_{L(INV)}$	V_S<V_{OUT}, V_{IN}=5V, T_A=25℃		12		A
V_S clamp voltage	V_{CLAMP}	I_S=20 mA	70	75		V
Supply current in sleep	I_{SLEEP}	V_S=48V, V_{IN}=V_{OUT}=V_{DEN}=0V, T_j =25℃		5.0	10	μA
		V_S =48V, V_{IN}=V_{OUT}=V_{DEN} =0V, T_j= 125℃			25	μA
Sleepy mode blanking time	t_{D_SLEEP}	V_S=48V, V_{IN}=V_{OUT}=0V V_{DEN}=5V to 0V	150	400	800	us
Supply current in active	$I_{S(ACTIVE)}$	V_S=48V, V_{DEN}=5V, $V_{IN0,1}$=0V,		1.2	2.5	mA
Control stage current consumption in ON state	$I_{GND(ON)}$	V_S=48V, V_{DEN}=5V, $V_{IN0,1}$=5V		5.0	10	mA
Off-state output current	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_S=60V, T_j =25℃		10	20	μA
		V_{IN} =V_{OUT}=0V, V_S=60V, T_j =125℃			50	μA
OUT - V_S diode voltage	V_F	I_{OUT} =-2A, T_j =150℃			0.9	V

Switching

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	V_S=48V,V_{DEN}=5V,R_L=10Ω		10	40	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$			30	100	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	V_S=48V,V_{DEN}=5V,R_L=10Ω	0.5	1.0	2.0	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		0.5	1.5	3.0	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	V_S=48V,V_{DEN}=5V,R_L=10Ω	-50		50	us

Logic input (IN, DEN)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_{LOW}				0.9	V
Low level logic input current	I_{LOW}	V_{LOW}=0.9V	2	11	35	uA
Logic input high level voltage	V_{HIGH}		2.1		6.0	V
High level logic input current	I_{HIGH}	V_{HIGH}=2.0V	1	10	32	uA

Logic input hysteresis voltage	$V_{(hyst)}$			0.2		V

Protections

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CL-pin voltage V_{CL} (in ON- state)	V_{CL}	V_S=48V, V_{DEN}=5V		0.6		V
Allowed I_{CL} range for adjusting current limit threshold	$I_{CL-range}$	V_S=48V, V_{DEN}=5V	6		120	uA
CL short to device ground current	$I_{CL-short}$	V_S=48V, V_{DEN}=5V	-50%	360	+50%	uA
DC short circuit current	I_{LIMH}	12V < V_S< 58V	40	50	60	A
		V_S=48V, V_{DEN}=5V, R_{CL}=5.6K	-25%	40	+25%	
		V_S=48V, V_{DEN}=5V, R_{CL}=8.6K	-25%	30	+25%	
		V_S=48V, V_{DEN}=5V, R_{CL}=16.8K	-25%	21	+25%	
		V_S=48V, V_{DEN}=5V, R_{CL}=34.8K	-25%	12	+25%	
		V_S=48V, V_{DEN}=5V, R_{CL}=94.7K	-25%	9	+25%	
Short circuit current during thermal cycling	I_{LIML}	V_S=48V, V_{DEN}=5V, T_R<T_j<T_{TSD},		15		
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Current limit reset temperature	T_R			135		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃		60		℃
Turn-off output voltage clamp	V_{DEMAG}	I_{OUT}=1A, V_{DEN}=5V, L= 3mH, T_j =-40℃ to 150℃	V_S-68	V_S-73		V

Current sense characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
I_{OUT}/I_{IS}	K_0	I_{OUT}=50mA, V_{DEN}=5V	-10%	2350	+10%	
I_{OUT}/I_{IS}	K_1	I_{OUT}=0.5A, V_{DEN}=5V	-5%	4800	+5%	
I_{OUT}/I_{IS}	K_2	I_{OUT}=2A, V_{DEN}=5V	-3%	5200	+3%	
I_{OUT}/I_{IS}	K_3	I_{OUT}=4A, V_{DEN}=5V	-3%	5200	+3%	
I_{OUT}/I_{IS}	K_4	I_{OUT}=10A, V_{DEN}=5V	-3%	5200	+3%	
K derating with temperature	ΔK		-2%	0	+2%	
Current sense leakage current	I_{IS0}	IS disabled: V_{DEN} =0V	0		1	uA
		IS enabled: V_{DEN} = 5V, channel ON, I_{OUT} = 0A		5		
Output voltage for IS shutdown	V_{OUT_MSD}	V_{DEN}=5V, R_{SENSE}=3.9K, V_{IN}=5V; I_{OUT}=6A		5		V
Max analog sense output voltage	V_{IS}	V_S=48V, V_{IS} =5V	4.5			V
Current sense output current in fault condition	I_{ISH}	V_S=48V, V_{IS} =5V	10	20	30	mA
Current sense output voltage in fault condition	V_{ISH}	V_S=48V, V_{IS} =5V	5.4	6	6.6	V

OFF-state diagnostic

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load voltage detection threshold	V_{OL}	V_{DEN}=5V, V_{IN}=0V	2	3.5	5	V
OFF-state output sink current	$I_{L(off2)}$	V_S=48V,V_{IN} = 0V, V_{OUT}=V_{OL}, T_j = -40℃ to 150℃		-50		uA
OFF-state diagnostic delay time from falling edge of IN	t_{DSTKON}	V_{DEN}=5V, V_{IN}= 5V to 0V, V_{OUT} =4V,	150	400	800	us
Settling time for valid OFF-state open load diagnostic indication from rising edge of DEN	$t_{D\_OL\_V}$	V_{IN}=0V, V_{OUT}=4V, V_{DEN}=0V to 5V			150	us
OFF-state diagnostic delay time from rising edge of V_{OUT}	t_{D_VOL}	V_{DEN}=5V,V_{IN}=0V, V_{OUT}=0V to 4V		5	30	us

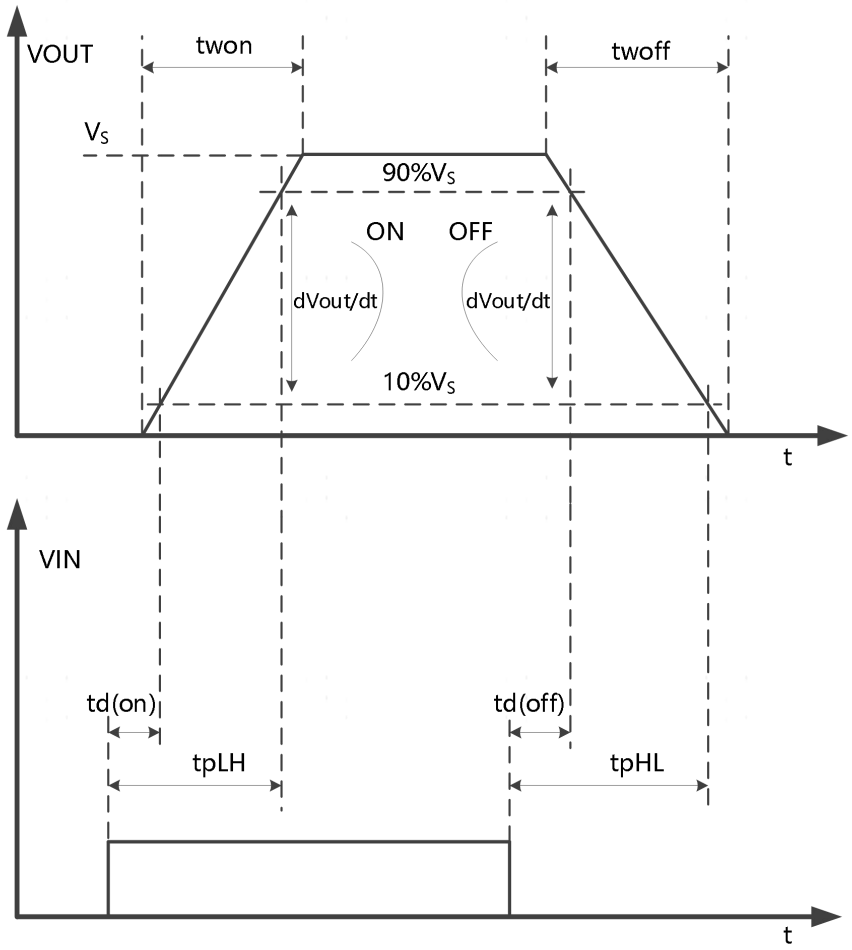
Current sense timings

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current sense settling time from rising edge of DEN	$t_{DSENSE1H}$	V_{IN}=5V, V_{DEN}=0V to 5V, R_{SENSE}=1K, R_L=10Ω			100	us
Current sense disable delay time from falling edge of DEN	$t_{DSENSE1L}$	V_{IN}=5V, V_{DEN}=5V to 0V, R_{SENSE}=1K, R_L=10Ω		5	20	us
Current sense settling time from rising edge of IN	$t_{DSENSE2H}$	V_{IN}=0V to 5V, V_{DEN}=5 V, R_{SENSE} =1K, R_L=10Ω		80	250	us
Current sense settling time from rising edge of I_{OUT}(dynamic response to a step change of I_{OUT})	$\Delta t_{DSENSE2H}$	V_{IN}=5V, V_{DEN}=5V, R_{SENSE}=1K, I_{IS}=90% of I_{IS_MAX}, I_{OUT} = 90% of I_{OUTMAX} R_L=10Ω			150	us
Current sense turn-off delay time from falling edge of IN	$t_{DSENSE2L}$	V_{IN}=5V to 0V, V_{DEN}=5V, R_{SENSE}=1K, R_L=10Ω		80	250	us

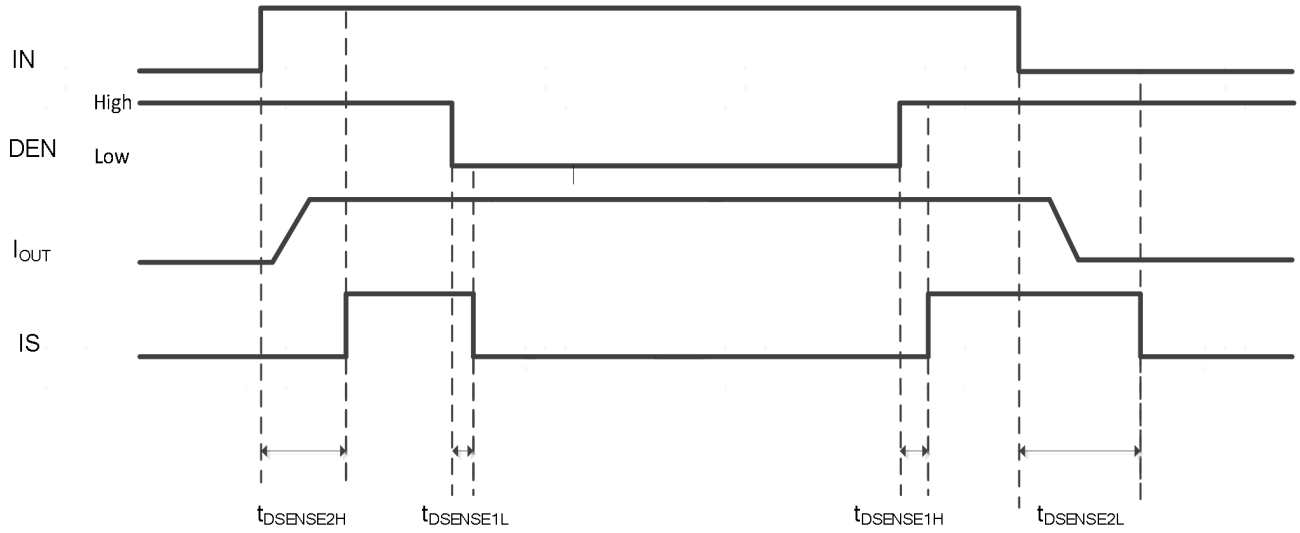
Note8: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew



Current sense timings (current sense mode)



T_{DSTKON}

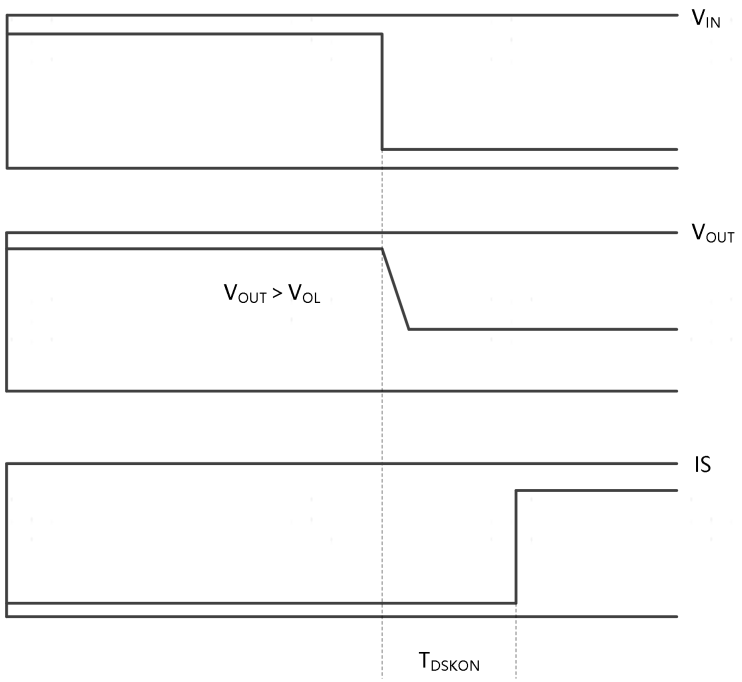


Table 2. Truth table

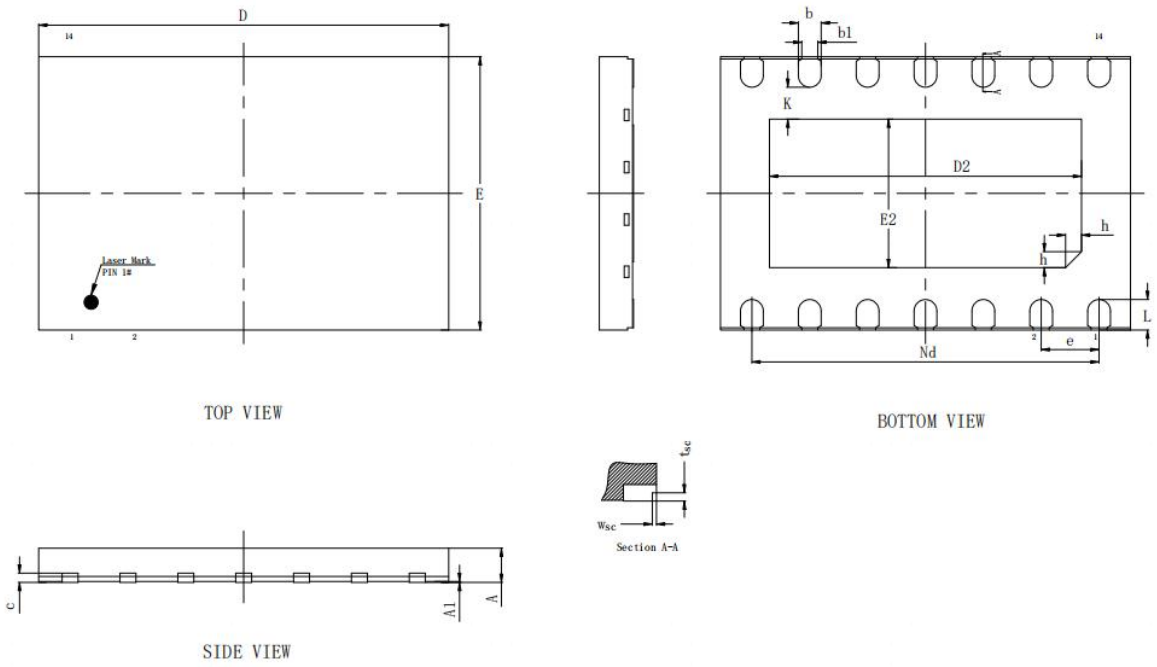
Conditions	IN	DEN	OUT	IS
Standby	L	L	L	0
Normal	L	H	L	0
	H	H	H	$I_{IS} = I_{OUT}/K$
Overload	H	H	H	I_{ISH}
OverTemperature	L	H	L	0
	H	H	L	I_{ISH}
Undervoltage	X	X	L	0
Short to V_S	L	H	H	I_{ISH}
	H	H	H	<Normal
Open-Load	L	H	H	I_{ISH}
Short circuit to GND	H	H	L	I_{ISH}

Table 3. Current sense output

DEN	MUX Channel	Current sense output			
		Normal	Overload	OFF-state	Negative output
L		Hi-Z			
H	Channel diagnostic	$I_{IS} = I_{OUT}/K$	$I_{IS} = I_{ISH}$	$I_{IS} = I_{ISH}$	Hi-Z

Package Outline

DFN9×6-14L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.45	0.50	0.55
b1		0.35REF	
c		0.203REF	
D	8.90	9.00	9.10
D2	6.75	6.85	6.95
e		1.27BSC	
Nd		7.62BSC	
E	5.90	6.00	6.10
E2	3.16	3.26	3.36
L	0.62	0.67	0.72
h	0.30	0.35	0.40
K		0.70REF	
W_{SC}	0.01	-	0.09
t_{SC}	0.08	-	0.18

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