Product Overview

The NSI824x devices are high reliability quad-channel digital isolators. The NSI824x device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI824x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSI824x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI824x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V$_{rms}$ Insulation voltage
- Data rate: DC to 100Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 200kV/us
- Chip level ESD: HBM: ±8kV
- Robust Electromagnetic Compatibility (EMC)
  – System-Level ESD, EFT, and Surge Immunity
  – Low Emissions
- Default output high level or low-level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -55℃~125℃
- RoHS-compliant packages:
  – SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V$_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	*Package*	*Body Size*
NSI824xWx-DSWR	SOP16(300mil)	10.30mm × 7.50mm
NSI824xCx-DSWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

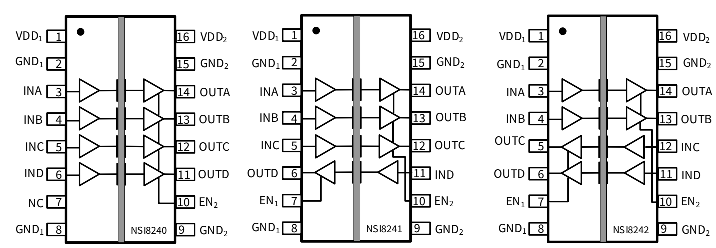

Figure 1. NSI824x Block Diagram

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1. Pin Configuration and Functions

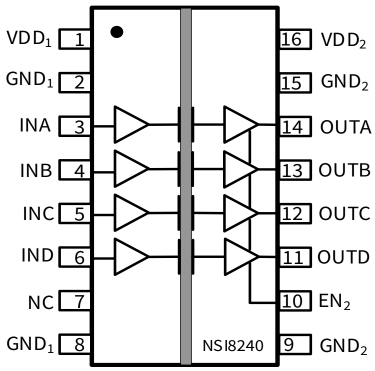

Figure 1.1 NSI8240 Package

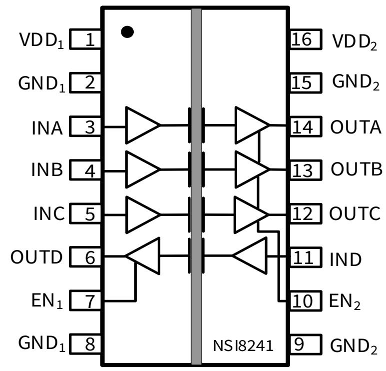

Figure 1.2 NSI8241 Package

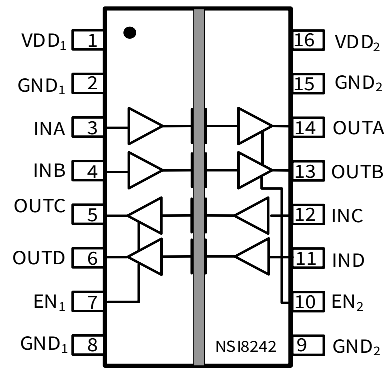

Figure 1.3 NSI8242 Package

Table 1.1 NSI824x Pin Configuration and Description

NSI8240 PIN NO.	*NSI8241 PIN NO.*	*NSI8242 PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD_1	Power Supply for Isolator Side 1
2	2	2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	3	3	INA	Logic Input A
4	4	4	INB	Logic Input B
5	5	12	INC	Logic Input C
6	11	11	IND	Logic Input D
7	7	7	NC/ EN_1	No Connection. Or Output Enable 1. Active high logic input. When EN_1 is high or NC, the output of Side 1 is enabled. When EN_1 is low, the output of Side 1 is disabled to high impedance state.
8	8	8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	9	9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	10	10	EN_2	Output Enable 2. Active high logic input. When EN_2 is high or NC, the output of Side 2 is enabled. When EN_2 is low, the output of Side 2 is disabled to high impedance state.
11	6	6	OUTD	Logic Output D
12	12	5	OUTC	Logic Output C
13	13	13	OUTB	Logic Output B
14	14	14	OUTA	Logic Output A
15	15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	16	VDD2	Power Supply for Isolator Side 2

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2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	VINA, VINB, VINC, VIND, VOUTA, VOUTB, VOUTC, VOUTD	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Operating Temperature	Topr	-55		125	℃	
Junction Temperature	T_j			150	℃	
Storage Temperature	Tstg	-65		150	℃	

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±2000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

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4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	Topr	-55		125	℃
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			100	Mbps

5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	78.9	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC（top）}$	41.6	℃/W
Junction-to-board thermal resistance	θ_{JB}	43.6	℃/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD_{POR}	2	2.2	2.4	V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V_{IT+}		1.5	2	V	
Falling input switching threshold	V_{IT-}	0.8	1.15		V	
Input threshold voltage hysteresis	$V_{I(HYS)}$		0.35		V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	I_{OH} =- 4mA

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Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 4mA
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		5	10	uA	
Start Up Time after POR	trbs		22	32	us	
Common Mode Transient Immunity	CMTI	±150	±200		kV/us	See Figure 6.11 , C_L = 15pF

6.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8240**					
	I_{DD1}(Q0)		1.48	1.83	mA	All Input 0V for NSI8240x0 Or All Input at supply for NSI8240x1
	I_{DD2}(Q0)		4.28	4.83	mA	
	I_{DD1}(Q1)		6.20	7.07	mA	All Input at supply for NSI8240x0 Or All Input 0V for NSI8240x1
	I_{DD2}(Q1)		4.30	5.01	mA	
	I_{DD1}(1M)		3.93	4.54	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		4.37	5.10	mA	
	I_{DD1}(10M)		4.16	4.83	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		5.80	6.55	mA	
	I_{DD1}(100M)		4.77	6.77	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		26.39	28.33	mA	
	NSI8241					
	I_{DD1}(Q0)		2.18	2.58	mA	All Input 0V for NSI8241x0 Or All Input at supply for NSI8241x1
	I_{DD2}(Q0)		3.58	4.08	mA	
	I_{DD1}(Q1)		5.72	6.55	mA	All Input at supply for NSI8241x0 Or All Input 0V for NSI8241x1
	I_{DD2}(Q1)		4.77	5.52	mA	
	I_{DD1}(1M)		4.04	4.68	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		4.26	4.96	mA	
	I_{DD1}(10M)		4.57	5.26	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		5.39	6.12	mA	
	I_{DD1}(100M)		10.17	12.16	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		20.98	22.94	mA	
	NSI8242					
	I_{DD1}(Q0)		2.88	3.33	mA	All Input 0V for NSI8242x0 Or All Input at supply for NSI8242x1
	I_{DD2}(Q0)		2.88	3.33	mA	
	I_{DD1}(Q1)		5.25	6.04	mA	

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I_{DD2}(Q1)		5.25	6.04	mA	All Input at supply for NSI8242x0 Or All Input 0V for NSI8242x1
	I_{DD1}(1M)		4.15	4.82	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		4.15	4.82	mA	
	I_{DD1}(10M)		4.98	5.69	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		4.98	5.69	mA	
	I_{DD1}(100M)		15.58	17.55	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		15.58	17.55	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	**NSI8240**					
	I_{DD1}(Q0)		1.19	1.56	mA	All Input 0V for NSI8240x0 Or All Input at supply for NSI8240x1
	I_{DD2}(Q0)		3.93	4.50	mA	
	I_{DD1}(Q1)		5.84	6.73	mA	All Input at supply for NSI8240x0 Or All Input 0V for NSI8240x1
	I_{DD2}(Q1)		3.94	4.67	mA	
	I_{DD1}(1M)		3.58	4.22	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		3.98	4.70	mA	
	I_{DD1}(10M)		3.82	4.51	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		4.92	5.65	mA	
	I_{DD1}(100M)		4.94	6.07	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		17.08	18.75	mA	
	NSI8241					
	I_{DD1}(Q0)		1.87	2.29	mA	All Input 0V for NSI8241x0 Or All Input at supply for NSI8241x1
	I_{DD2}(Q0)		3.24	3.76	mA	
	I_{DD1}(Q1)		5.36	6.21	mA	All Input at supply for NSI8241x0 Or All Input 0V for NSI8241x1
	I_{DD2}(Q1)		4.41	5.18	mA	

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I_{DD1}(1M)		3.68	4.34	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		3.88	4.58	mA	
	I_{DD1}(10M)		4.09	4.79	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		4.64	5.36	mA	
	I_{DD1}(100M)		7.97	9.24	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		14.04	15.58	mA	
	NSI8242					
	I_{DD1}(Q0)		2.56	3.03	mA	All Input 0V for NSI8242x0 Or All Input at supply for NSI8242x1
	I_{DD2}(Q0)		2.56	3.03	mA	
	I_{DD1}(Q1)		4.89	5.70	mA	All Input at supply for NSI8242x0 Or All Input 0V for NSI8242x1
	I_{DD2}(Q1)		4.89	5.70	mA	
	I_{DD1}(1M)		3.78	4.46	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		3.78	4.46	mA	
	I_{DD1}(10M)		4.37	5.08	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		4.37	5.08	mA	
	I_{DD1}(100M)		11.00	12.41	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		11.00	12.41	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	**NSI8240**					
	I_{DD1}(Q0)		1.17	1.53	mA	All Input 0V for NSI8240x0 Or All Input at supply for NSI8240x1
	I_{DD2}(Q0)		3.71	4.35	mA	
	I_{DD1}(Q1)		5.74	6.52	mA	All Input at supply for NSI8240x0 Or All Input 0V for NSI8240x1
	I_{DD2}(Q1)		3.86	4.50	mA	
	I_{DD1}(1M)		3.50	4.05	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		3.86	4.49	mA	

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I_{DD1}(10M)		3.68	4.22	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		4.56	5.20	mA	
	I_{DD1}(100M)		4.66	5.16	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		13.58	15.60	mA	
	NSI8241					
	I_{DD1}(Q0)		1.80	2.23	mA	All Input 0V for NSI8241x0 Or All Input at supply for NSI8241x1
	I_{DD2}(Q0)		3.07	3.64	mA	
	I_{DD1}(Q1)		5.27	6.01	mA	All Input at supply for NSI8241x0 Or All Input 0V for NSI8241x1
	I_{DD2}(Q1)		4.33	5.00	mA	
	I_{DD1}(1M)		3.59	4.16	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		3.77	4.38	mA	
	I_{DD1}(10M)		3.90	4.46	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		4.34	4.95	mA	
	I_{DD1}(100M)		6.89	7.77	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		11.35	12.99	mA	
	NSI8242					
	I_{DD1}(Q0)		2.44	2.94	mA	All Input 0V for NSI8242x0 Or All Input at supply for NSI8242x1
	I_{DD2}(Q0)		2.44	2.94	mA	
	I_{DD1}(Q1)		4.80	5.51	mA	All Input at supply for NSI8242x0 Or All Input 0V for NSI8242x1
	I_{DD2}(Q1)		4.80	5.51	mA	
	I_{DD1}(1M)		3.68	4.27	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		3.68	4.27	mA	
	I_{DD1}(10M)		4.12	4.71	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		4.12	4.71	mA	
	I_{DD1}(100M)		9.12	10.38	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		9.12	10.38	mA	

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6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		12.0	18	ns	See Figure 6.9 , C_L = 15pF
	t_{PHL}		12.5	18	ns	See Figure 6.9 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.9 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.9 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.9 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	
Disable high to Tri-State	t_{PHZ}		8.67	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Enable to Data high Valid	t_{PZH}		8.75	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Disable low to Tri-State	t_{PLZ}		7.7	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Enable to Data low Valid	t_{PZL}		9.5	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		12.85	19	ns	See Figure 6.9 , C_L = 15pF
	t_{PHL}		12.60	19	ns	See Figure 6.9 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.9 , C_L = 15pF

Rising Time	t_r			5.0	ns	See Figure 6.9 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.9 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	
Disable high to Tri-State	t_{PHZ}		11	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Enable to Data high Valid	t_{PZH}		11.5	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Disable low to Tri-State	t_{PLZ}		9.3	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Enable to Data low Valid	t_{PZL}		12.3	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		13.97	20	ns	See Figure 6.9 , C_L = 15pF
	t_{PHL}		12.72	20	ns	See Figure 6.9 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.9 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.9 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.9 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	
Disable high to Tri-State	t_{PHZ}		13.9	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Enable to Data high Valid	t_{PZH}		15.6	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k

Disable low to Tri-State	t_{PLZ}		12.6	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k
Enable to Data low Valid	t_{PZL}		16.8	30	ns	See Figure 6.10 , C_L = 15pF, R_L=1k

6.8. Typical Performance Characteristics

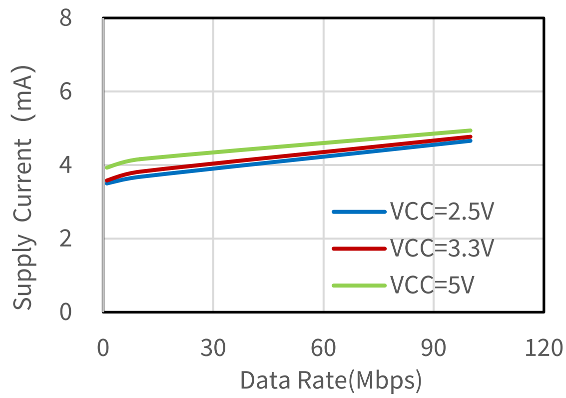

Figure 6.1 NSI8240 VDD1 Supply Current vs Data Rate

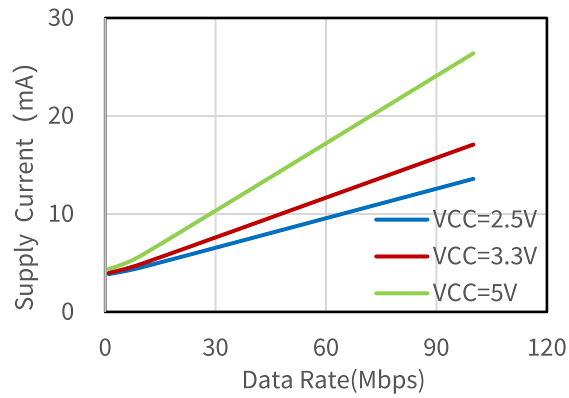

Figure 6.2 NSI8240 VDD2 Supply Current vs Data Rate

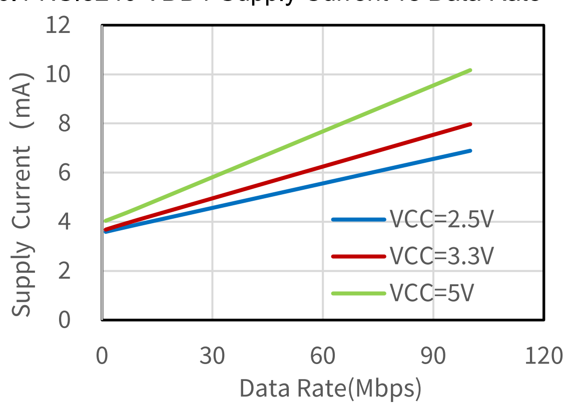

Figure 6.3 NSI8241 VDD1 Supply Current vs Data Rate

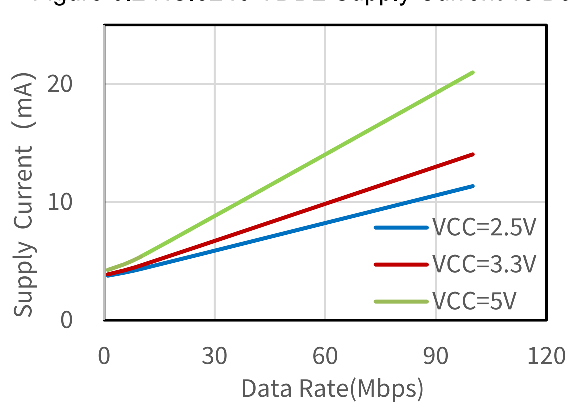

Figure 6.4 NSI8241 VDD2 Supply Current vs Data Rate

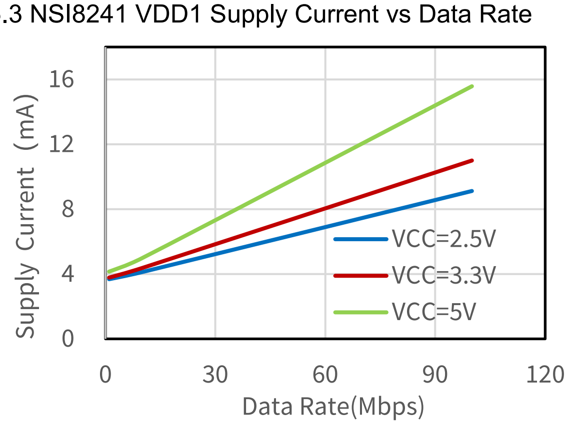

Figure 6.5 NSI8242 VDD1 Supply Current vs Data Rate

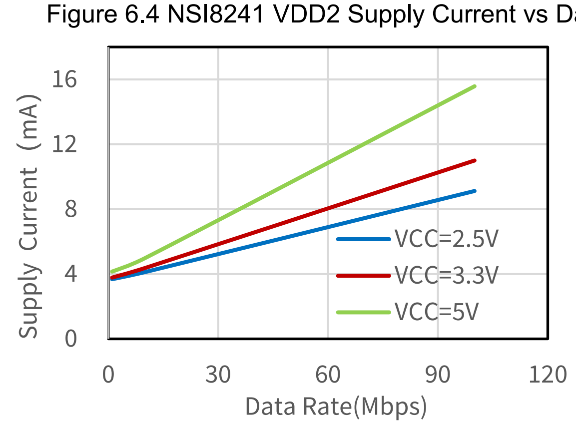

Figure 6.6 NSI8242 VDD2 Supply Current vs Data Rate

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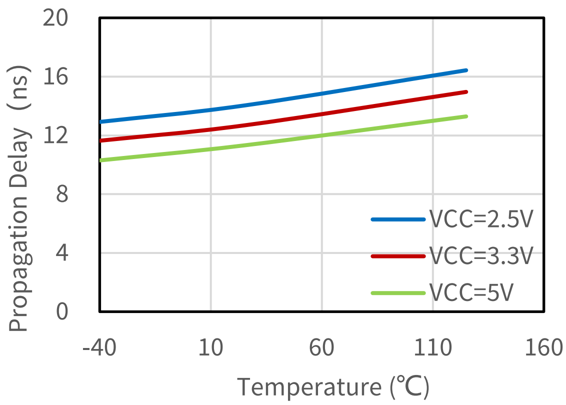

Figure 6.7 Rising Edge Propagation Delay Vs Temp

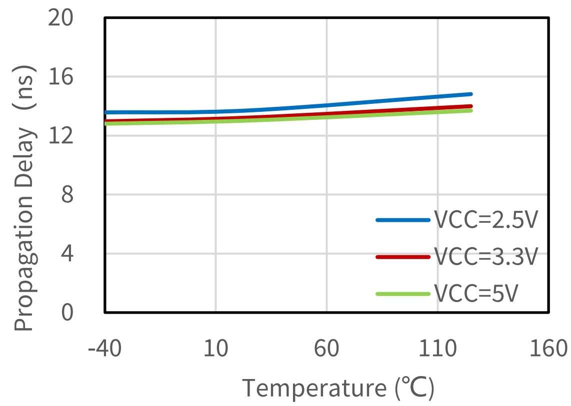

Figure 6.8 Falling Edge Propagation Delay Vs Temp

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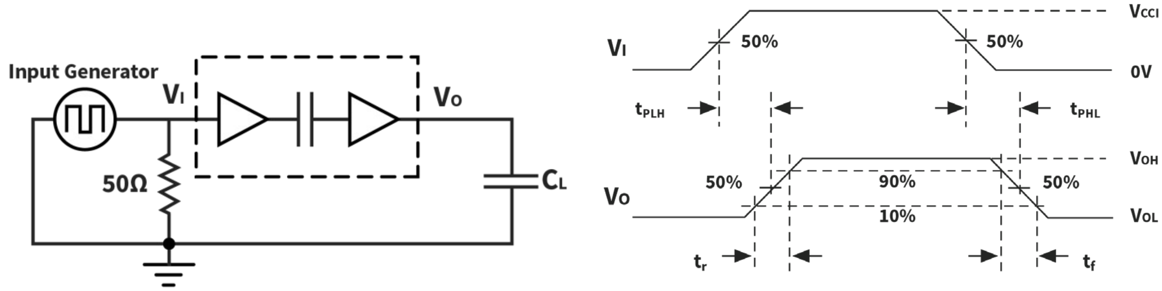
6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR ≤ 50kHz, tr ≤ 3ns, tf ≤ 3ns, Duty cycle = 50%, Zo = 50 Ω.

Figure 6.9 Switching Characteristics Test Circuit and Waveform

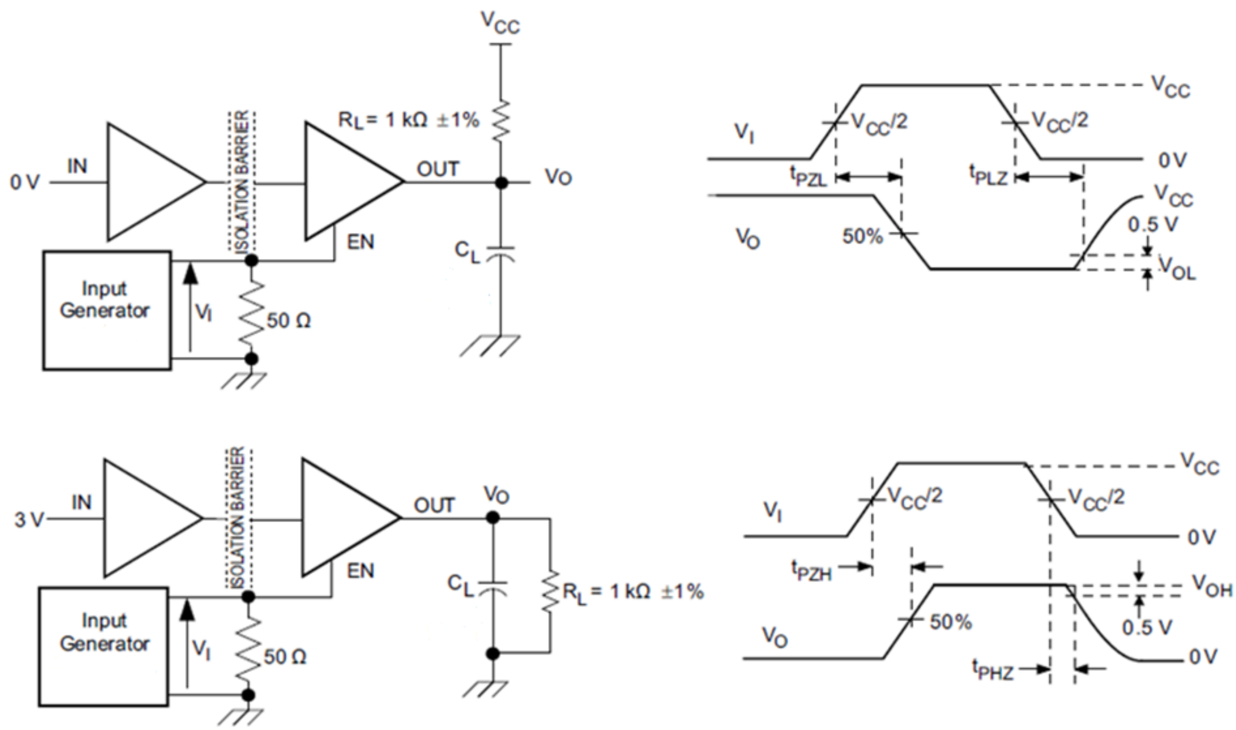


Figure 6.10 Enable/Disable Propagation Delay Time Test Circuit and Waveform

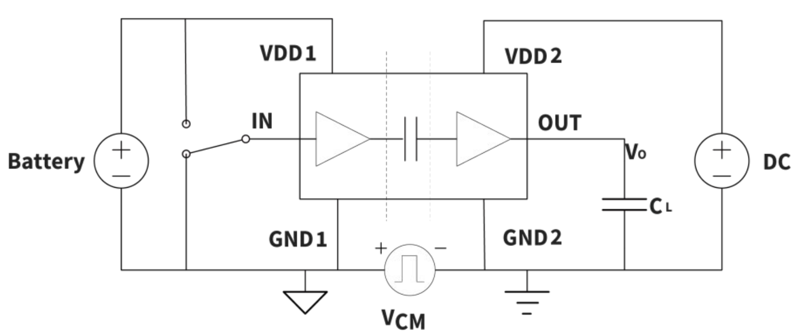


Figure 6.11 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value SOP16 (300mil)	Unit	Comments
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	24	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value SOP16 (300mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value SOP16 (300mil)	Unit
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}

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Description	Test Condition	Symbol	Value	Unit
			SOP16 (300mil)	
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s			pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	\	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s			pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.5*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us	V_{IOSM}	10000	V_{PEAK}

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Description	Test Condition	Symbol	Value	
			SOP16 (300mil)	Unit
	waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$			
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	$>10^{12}$	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	$>10^{11}$	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	$>10^{9}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	5000	V_{RMS}

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI824x-DSWR (SOP16(300mil))

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{θJA}$ = 78.9 °C/W[1)], T_J = 150 °C, T_A = 25 °C	1584	mW
Safety Supply Current	$R_{θJA}$ = 78.9 °C/ W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	316.8	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{θJA}$, of SOP16(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

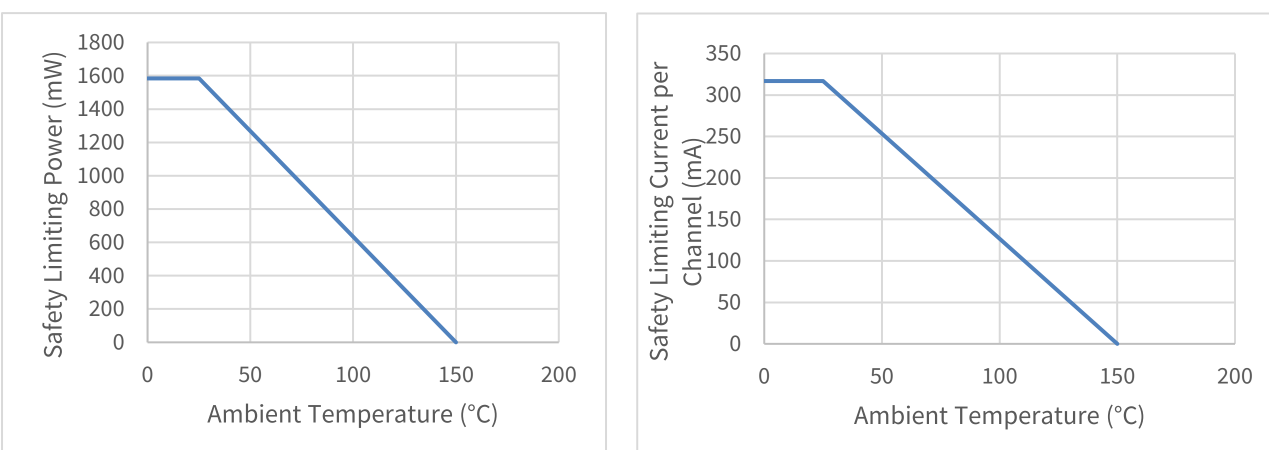

Figure 7.1 NSI824x Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17).

7.4. Regulatory Information

The NSI824xWx-DSWR are approved or pending approval by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022	Certified According to EN IEC 62368-1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation	5000Vrms for 1min
E500602	E500602	File (40052820)	CQC20001264939	R50574061

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8. Function Description

8.1. Overview

The NSI824x is a Quad-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI824x devices are high reliability quad-channel digital isolator. The NSI824x device is safety certified by UL1577 support $5kV_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI824x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSI824x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI824x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI824x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 7.1 Output status vs. power status

Input[1]	*ENx[2]*	*VDDIN status*	*VDDOUT status*	*Output*	*Comment*
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output Disabled, the output is high impedance
X	H or NC	Unready	Ready	L(NSI824xx0) H(NSI824xx1)	The output follows the same status with the input after input side VDD is powered on.
X	L	Unready	Ready	Z	Output Disabled, the output is high impedance
X	X	Ready	Unready	Undetermined	The output follows the same status with the input after output side VDD is powered on.

Note: H=Logic high; L=Logic low; X=Logic low or logic high

VDDIN is input side power; VDDOUT is output side power.

(1) There is a protection diode between the input and the VDDIN. When the VDDIN is floating, the strong drive signal through the input pin will put the VDDIN in an indeterminate state.

(2) The ENx is output side enable.

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8.2. OOK Modulation

NSI824x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1 to Figure 7.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

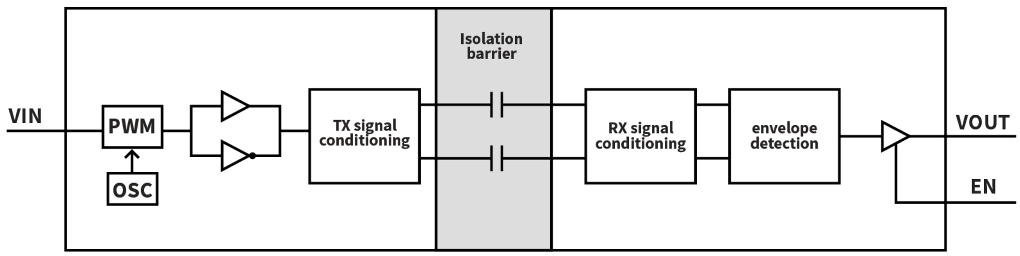

Figure 8.1 Single Channel Function Block Diagram

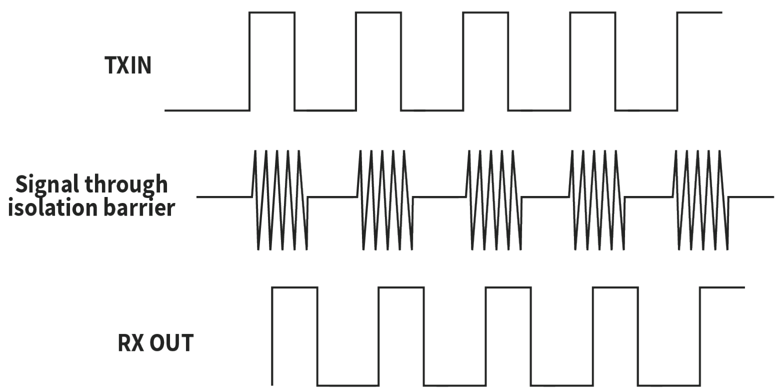

Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

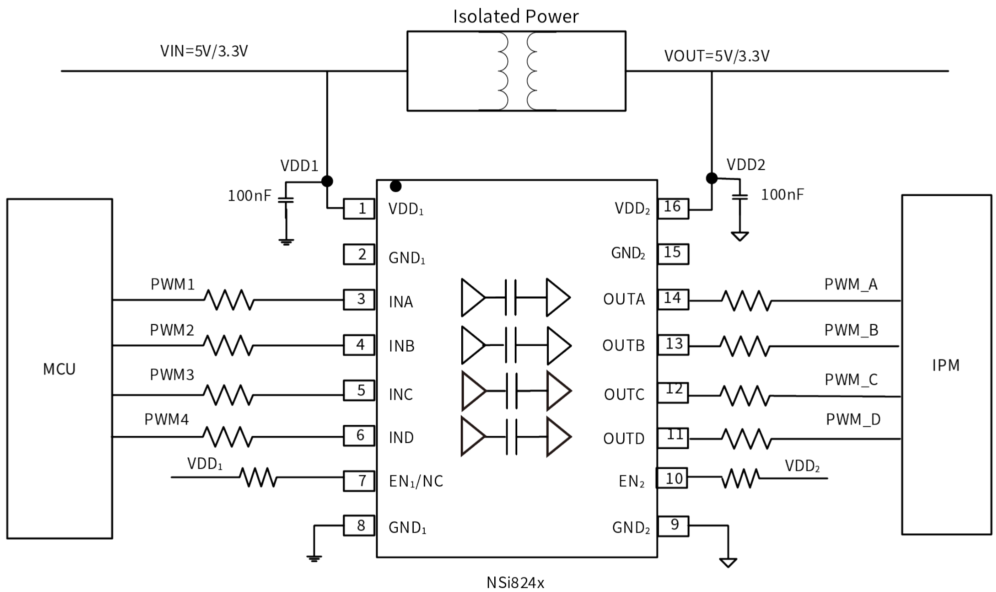

Figure 9.1 Typical PWM isolation circuit for IPM

9.2. PCB Layout

The NSI824x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

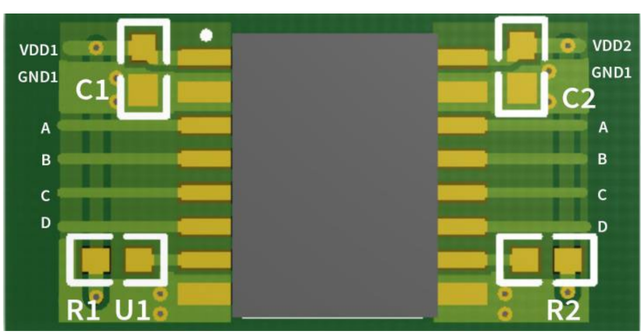

Figure9.2 Recommended PCB Layout — Top Layer

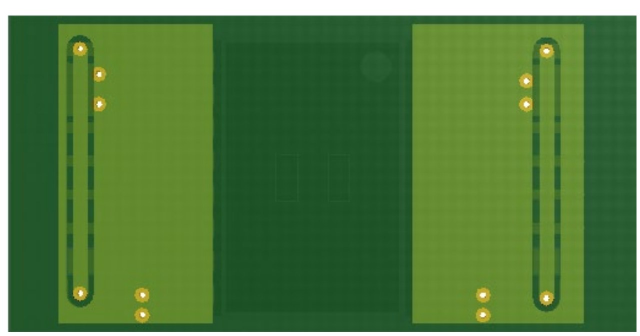

Figure9.3 Recommended PCB Layout — Bottom Layer

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9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI824x at 50Mbps data rate output. The result shows a typical measurement on NSI824x with low jitter and wide open eye characteristics.

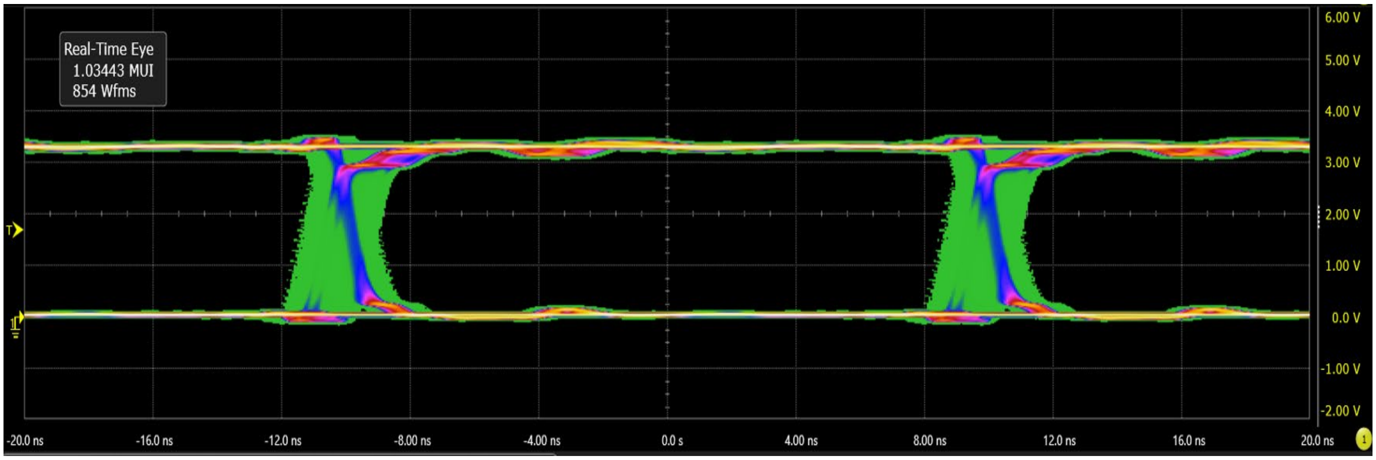

Figure 9.4 Eye Diagram at 50Mbps PRBS 2^{16}-1, 2.5V and 25℃

9.4. Typical Supply Current Equations

The typical supply current of NSI824x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF.

NSI8240:

I_{DD1} = 0.298 *a1+1.458*b1+0.878*c1.

I_{DD2} = 3.93+ 0.5*VDD2*f* C_L *c1*10^{-3}

When a1 is the channel number of default state input at side 1, b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1.

NSI8241:

I_{DD1} = 1.875 +1.16*b1+0.58*c1+ 0.5*VDD1*f* C_L *c2*10^{-3}

I_{DD2} = 3.245 +1.16*b2+0.58*c2+ 0.5*VDD2*f* C_L *c1*10^{-3}

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

NSI8242:

I_{DD1} = 2.56 +1.16*b1+0.58*c1+ 0.5*VDD1*f* C_L *c2*10^{-3}

I_{DD2} = 2.56 +1.16*b2+0.58 *c2+ 0.5*VDD2*f* C_L *c1*10^{-3}

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

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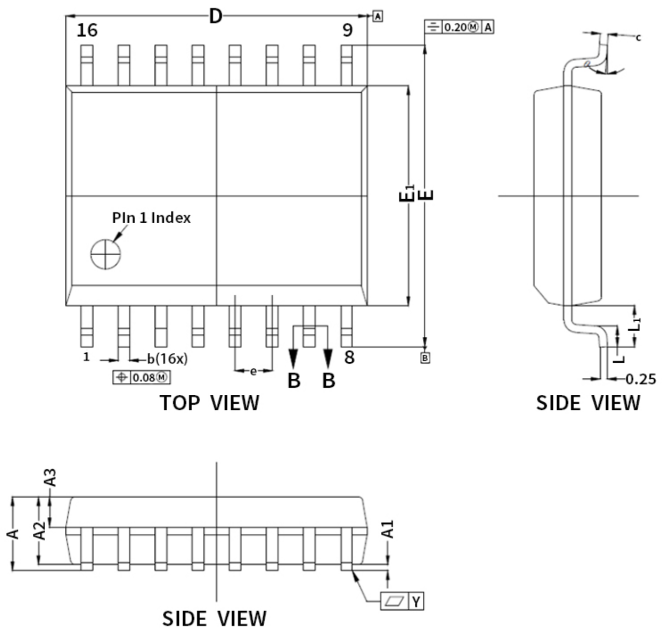
10. Package Information



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 10.1 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

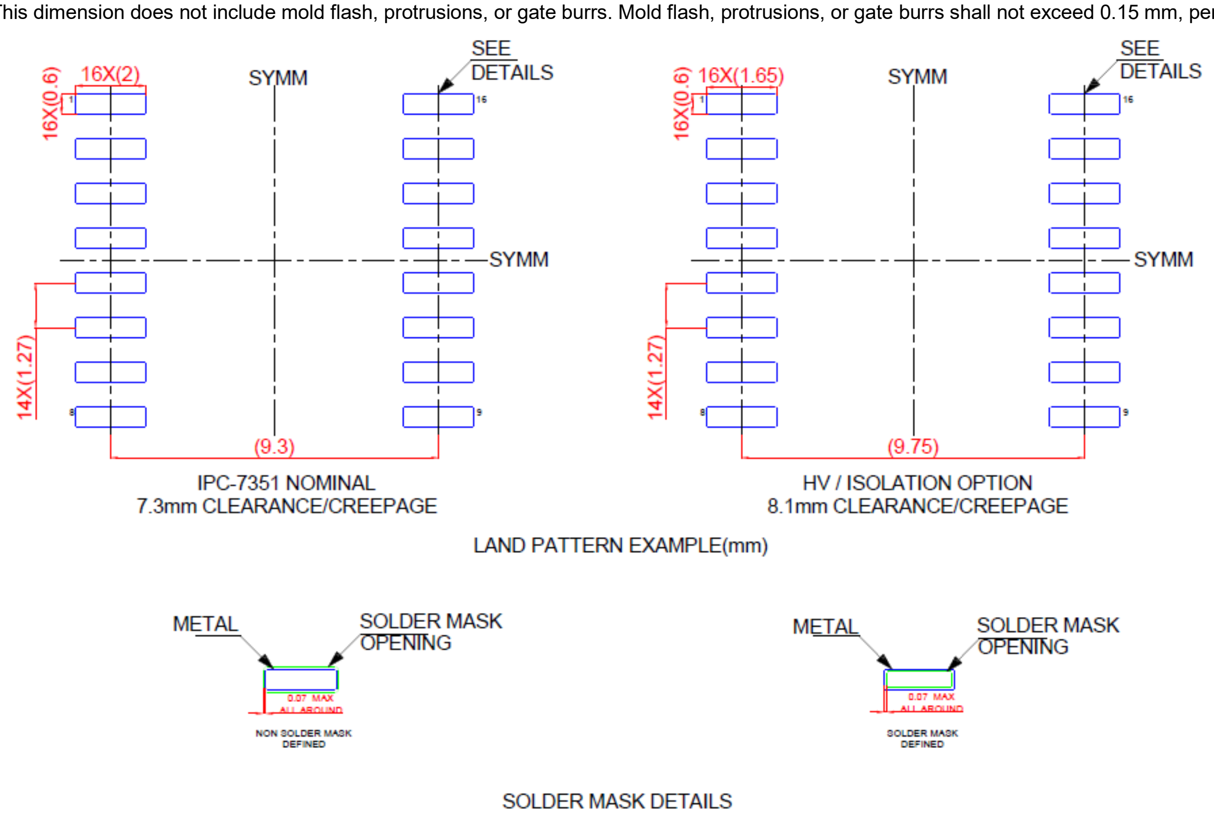


Figure 10.2 SOP16(300mil) SOW16 Package Board Layout Example

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11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8240W0-DSWR	5	4	0	100	Low	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8240W1-DSWR	5	4	0	100	High	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8241W0-DSWR	5	3	1	100	Low	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8241W1-DSWR	5	3	1	100	High	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8242W0-DSWR	5	2	2	100	Low	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8242W1-DSWR	5	2	2	100	High	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8240C0-DSWR	5	4	0	100	Low	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8240C1-DSWR	5	4	0	100	High	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8241C0-DSWR	5	3	1	100	Low	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8241C1-DSWR	5	3	1	100	High	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8242C0-DSWR	5	2	2	100	Low	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000
NSI8242C1-DSWR	5	2	2	100	High	-55 to 125℃	3	SOP16 (300mil)	SOW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

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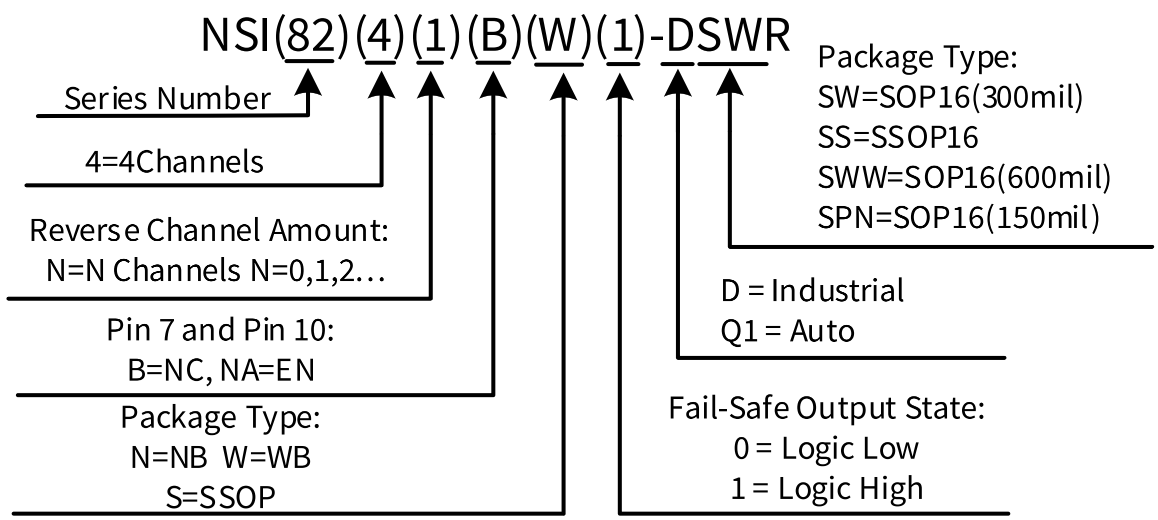
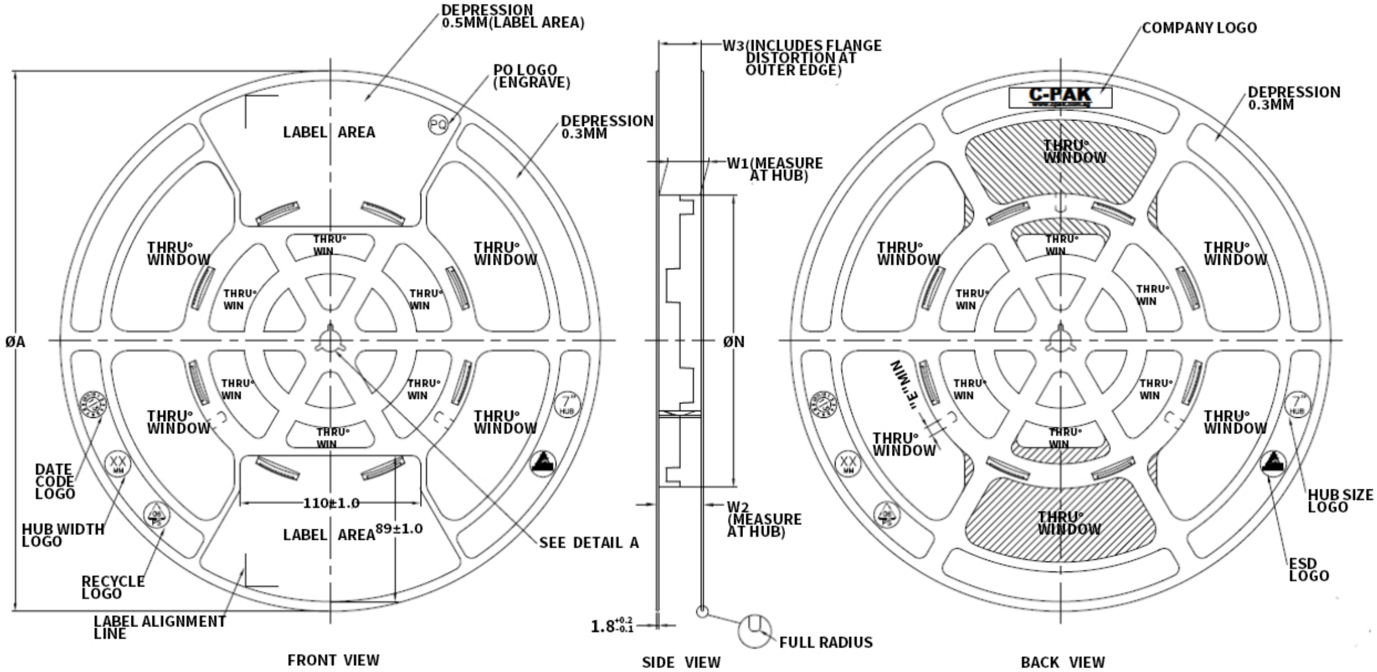
Part Number Rule:

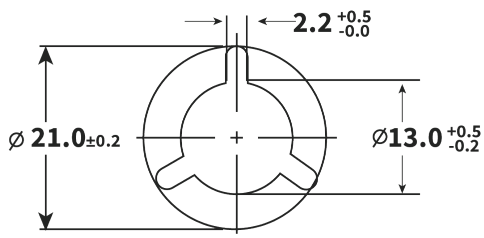


12. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI824x	tbd	tbd	tbd	tbd

13. Tape and Reel Information



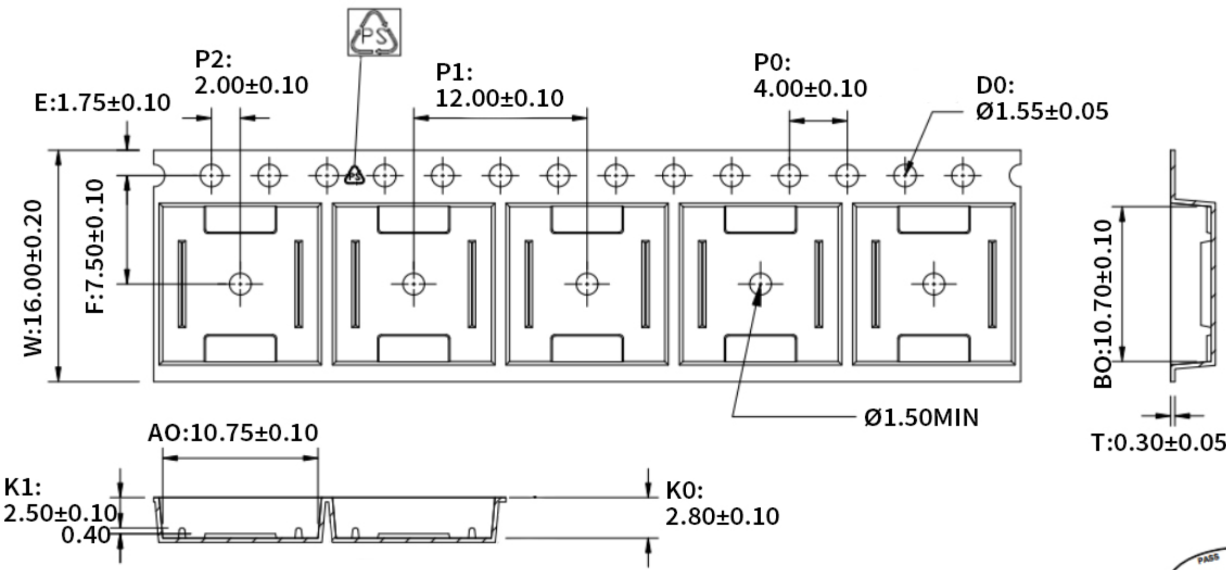


ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Reel Information (for all packages)



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:10^{5}~ 10^{10}Ω/口

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

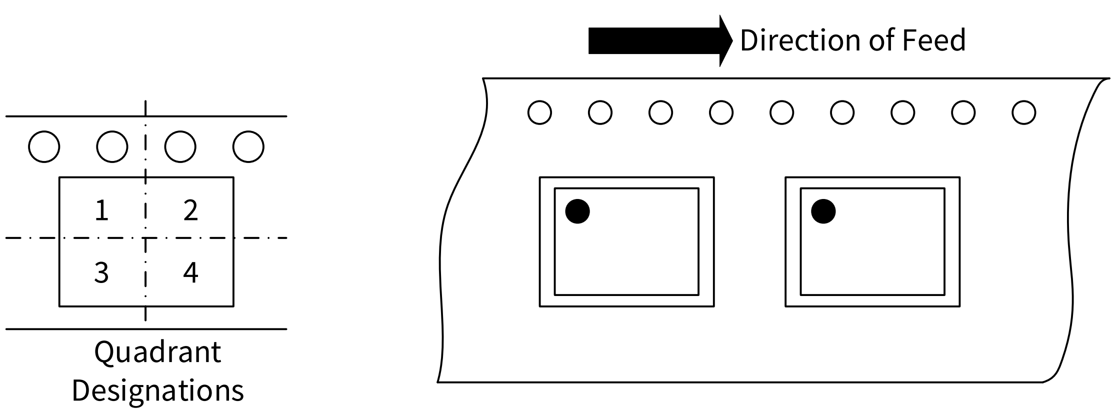


Figure 13.2 Tape Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial version	2020/11/13
1.1	Changed tape and reel information	2020/12/20
1.2	Operating temperature support -55 to 125 ℃	2021/7/7
1.3	Update Package Board Layout Example, update CQC information, Add SSOP16 package products	2021/12/29
1.4	Add SOP16 package products. Update SSOP16 Package Shape and Dimension in millimeters. Changed AEC-Q100 description. Update Part Number Rule, Package Board Layout Example. Update SOWW16 VISO. Update Regular Information NSI824xS-DSSR UL1577 file. Correct SOWW16 MSL.	2022/9/7
1.5	Update Typical Supply Current Equations	2023/2/7
1.6	Correct formatting and images. Update Input characteristics. Update Safety certification info throughout the document. Update eye diagram. Update Package Information. Update Function Description.	2025/1/13
1.7	Delete SOP16(150mil) /SSOP16/SOP16(600mil)package products. Update electrical characteristics. Update supply current characteristics at 2.5V/3.3V/5V. Update switching characteristics at 2.5V/3.3V/5V. Update Insulation and safety related specifications. Update regulatory Information. Update eye diagram.	2025/2/26
2.0	Add SOW16 package NSI824xCx products. Add Supply Current of NSI8240Wx. Update Supply Current of NSI8242Wx. Update Typical Supply Current Equations. Add Typical Performance Characteristics. Change MSL level.	2025/3/13

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